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OM

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PM 1 (B)

ECE

ACE ACADAMY

VLSI

sir: Narsimha Scientist CDRDO).

① JFET:

→ Book: Microelectronics ckts by Sedra & Smith (old edition).

- Construction and operation of JFET.
- Drain Char. & Transfer Characteristics.
- JFET biasing.
- Amplifiers Analysis.
- Frequency Analysis.

} Book Boyle sted.

② MOSFET:

→ Book: → Cmos VLSI Design by Weste & Harris (Ch-1, 2 & 4).

→ Design of Analog Cmos IC by RAZAVI (Ch: 2 & 3)

→ Depletion & Enhancement MOSFET.

→ Construction & operation of MOSFET.

→ Drain Char. & Transfer characteristics.

→ Mos Capacitor. ⊛

→ MOSFET Analysis.

→ Amplifier Analysis.

→ Frequency Analysis. ⊛

③ CMOS:

- Implementation of and functions in Cmos Technology.

- Transfer Charac. of an Inverter.
- Transistor sizing.
- Rise time, fall time, propogation Delay & Contamination Delay.
- Delay calculation.
- Power
- Noise Margin.

④ Device Technology:

- Ic fabrication technology:

Steps:

① oxidation.
② Diffussion.
③ Ion - implementation.
④ photolithography.

- n-tube (or) n-well.
- p-tube (or) p-well.
- Twin-tube (or) Double-well CMOS process.

☆ Energy Band in Si (silicon):

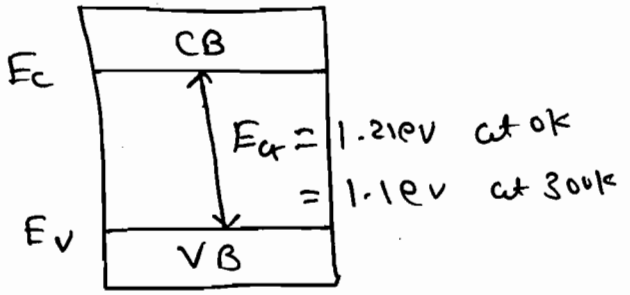
IMP Concept: Why silicon (Si)?

Ans:

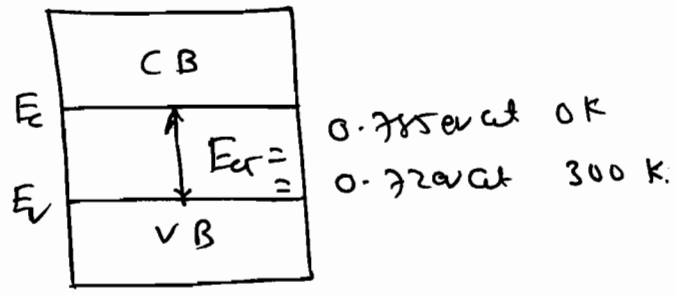
- Low leakage current.

I_o (Si) : nA
I_o (Ge) : μA
} I_o (Ge) ≅ 1000 I_o (Si).

- More energy gap.



Si



Ge

→ Carriers Concentration remain same for applied electric energy, it change only when thermal energy is applied.

- More Resistivity.

ρ_i (Ge) = 44.6 ≅ 45 Ω-cm

ρ_i (Si) = 231.5 K ≅ 230 K Ω-cm.

$$\rho_i = \frac{1}{n_i (\mu_p + \mu_n) q}$$

Si:

Millman: μ_n = 1300 $cm^2/V\text{-}s$
μ_p = ~~400~~ 500 $cm^2/$
$n_i = 1.5 \times 10^{10}$ $/cm^3$.

SMJ: μ_n = 1350 $cm^2/V\text{-}s$.
μ_p = 450 $cm^2/V\text{-}s$.

Ge: Millman

$\mu_n = 3800 \ cm^2/V\text{-}s$

$\mu_p = 1800 \ cm^2/V\text{-}s$

SMJ

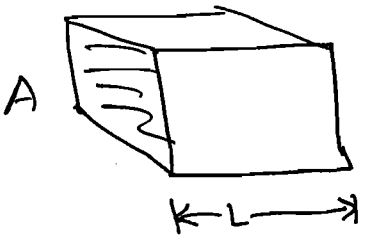
$\mu_n = 3900 \ cm^2/V\text{-}s$

$\mu_p = 1900 \ cm^2/V\text{-}s$

- More Resistance:

$$R_{(si)} = \frac{\rho_{(si)} L}{A}$$

$$R_{(ge)} = \frac{\rho_{(ge)} L}{A}$$



A & L same for the both.

$R_{(si)} > R_{(ge)}$.

So, more electron attenuation in si. So, Low leakage current in si.

- High Temp. (withstand).

Si → 1425°C

Ge → 936°C.

- High Voltage (sustained).

→ VLSI stands for very large Scale integration.

→ This is a field which involves integration (or) packing more & more devices in a smaller and smaller area.

⇒ All RF devices are made up of Gallium Arsenide (GaAs)

GaAs: $\mu_n = 8500 \text{ cm}^2/\text{V-s}$.

$\mu_p = 400 \text{ cm}^2/\text{V-s}$.

→ GaAs has high mobility for high current & High freq.

→ Si for Low and medium freq.

→ npn is used instead of pnp because high mobility of electron in npn Compared to pnp.

→ Bardeen, Brattain & Shockley was invented first transistor in 1948.

→ Schockely invented FET in 1952

→ Jack Killby invented IC in 1958.

→ Kahng & Atalla invented MOSFET in 1960.

→ Integrated circuit Consist of active & Passive devices & also interconnection in a integrated (or) Package on a Singie Crystal of a Si chip.

→ IC fabrication is a batch process that is more no. of CKTS & IC's can be fabricated at one go.

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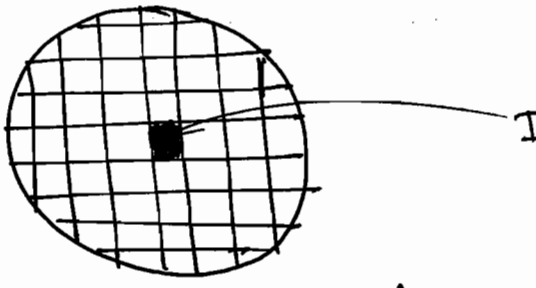


Water (100 to 800 IC's)

* Advantages of IC :

→ Smaller size.

→ Cost → Low

→ Low Power

→ High Speed

→ Reliable

→ Better performance.

→ miniaturization & hence increase the equipment density.

→ Cost reduction due to batch processing.

→ Increase Reliability due to elimination of Soldering joints.

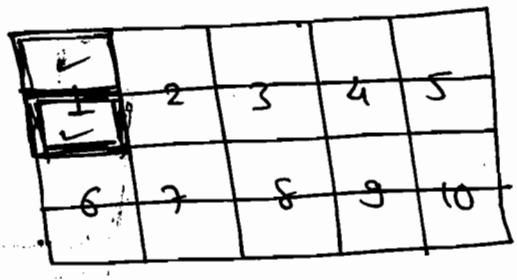
→ Improved function of performance i.e. Complex circuitary can be fabricated with better characteristics.

→ Increase operating speeds due to reduction of parasitics.

→ Reduction in power consumption.

→ In 1965 Gordon moore (founder of Intel) observed that transistor count becomes double for every 18 to 24 months.

→ $\frac{\text{Size}}{2} \Rightarrow \frac{\text{Area}}{2} = \frac{W}{\sqrt{2}} \times \frac{L}{\sqrt{2}}$



Scaling factor (s or α) $= \sqrt{2}$.

* Technology Scaling :- (in terms of channel engths): L

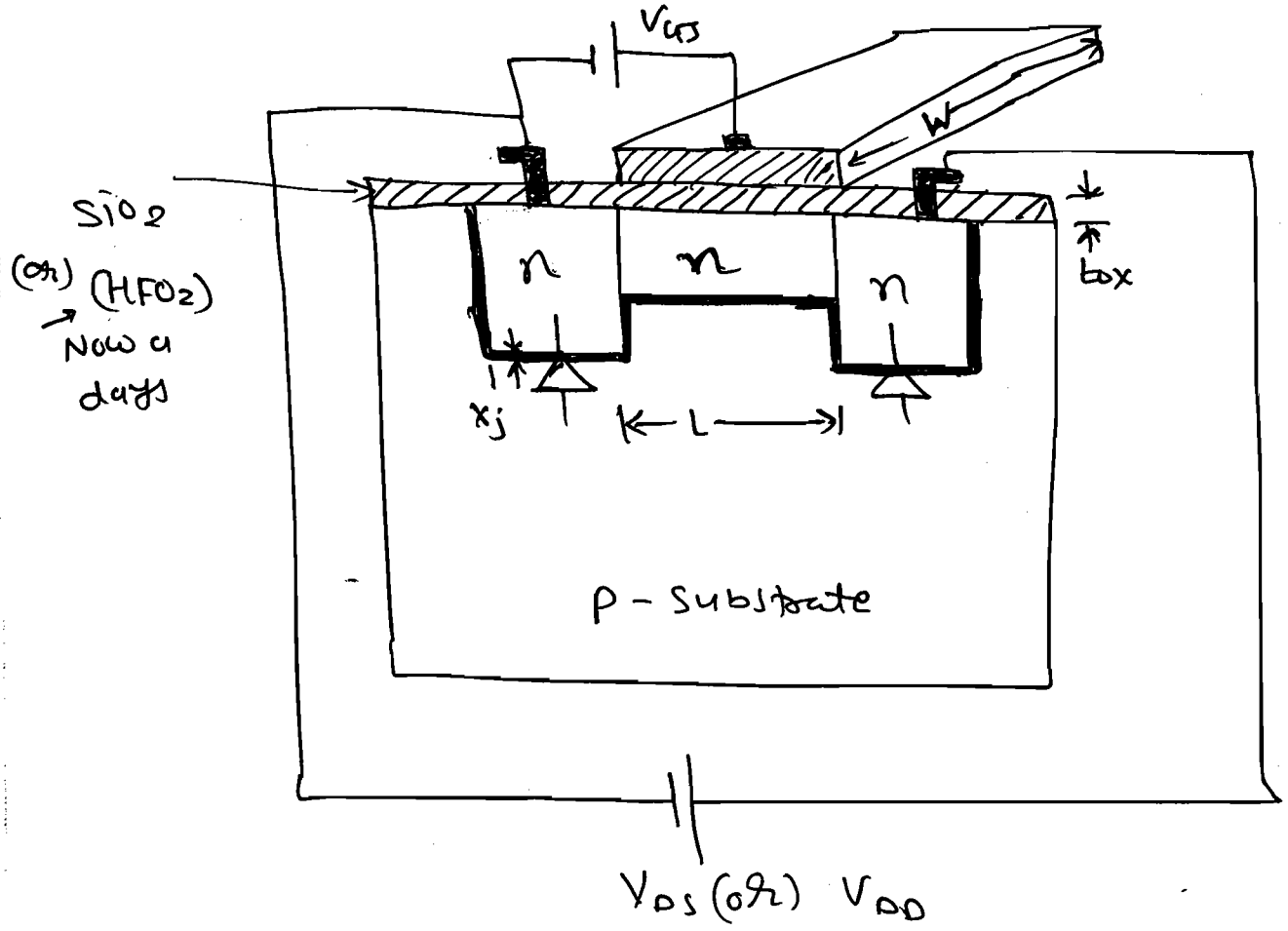
L = 10 μm (4004 μP) 1971	10 μm	180 nm
	6 μm	130 nm
	3 μm	90 nm
	1.5 μm	65 nm
	1 μm	45 nm
	0.8 μm	32 nm ↙
	0.6 μm	22 nm ↙ } now a days.
	0.35 μm	14 nm ↙
	0.25 μm	

→ Channel length (↑) = Leakage Current (or) (power) (↓).

* Scaling:

① Constant Field scaling.

② Constant Voltage scaling.



→ L = Channel Length.

→ W = Channel width.

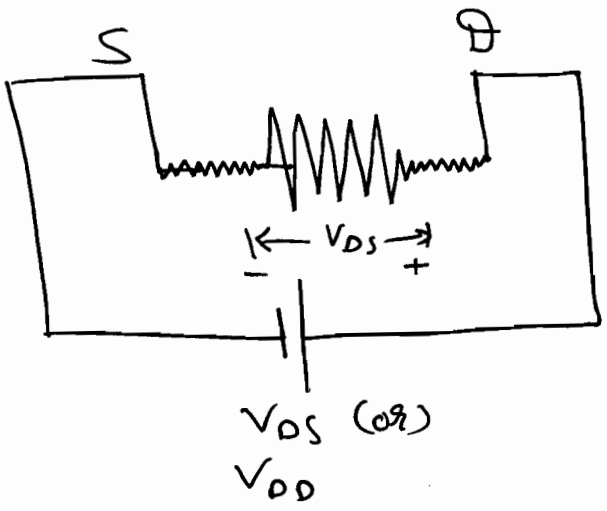
→ t_{ox} = Gate oxide thickness.

→ x_j = jn depletion thickness.

→ V_T = Threshold Voltage.

→ V_{DD} = power Supply Voltage.

→ N_A (or) N_D = Substrate Dopping Concentration. (or) density.



$$E = \frac{V_{DS}}{L}.$$

① Constant Field Scaling:

⇒

Parameter		Before scaling	After scaling.
①	Channel length	L	$L' = L/s$
②	Channel width	W	$W' = W/s.$
③	Gate oxide thickness	t_{ox}	$t_{ox}' = t_{ox}/s.$
④	junction depletion thickness	x_j	$x_j' = x_j/s.$
⑤	Threshold voltage	V_T	$V_T' = V_T/s.$
⑥	Power supply voltage	V_{DD}	$V_{DD}' = V_{DD}/s.$
⑦	Substrate doping density	N_A (or) N_D	$N_A' = sN_A$ (or) $N_D' = sN_D$

$$W \propto \sqrt{\left(\frac{1}{N_A} + \frac{1}{N_D}\right)}.$$

② Constant Voltage Scaling:

Parameter	Before Scaling	After Scaling.
① Channel length	L	$L' = L/S$.
② Channel width	W	$W' = W/S$.
③ Gate oxide thickness	t_{ox}	$t_{ox}' = t_{ox}/S$.
④ junction depletion thickness	x_j	$x_j' = x_j/S$.
⑤ Threshold Voltage	V_T	V_T
⑥ Supply Voltage	V_{DD}	V_{DD}.
⑦ Substrate dopping density	N_A (or) N_D	Remain unchanged $N_A' = S^2 N_A$ $N_D' = S^2 N_D$.

* Level's of Integration:

① SSI: Such as 7404 has upto 10 Gates per chip.

ex: logic gates, flip-flop.

② MSI: Such as 7416 counter have upto 1000 gates per chip.

ex: Counters ICs, multiplexers, Adders.

③ LSI: Such as simple 8-bit µp have upto 10,000 gates per chip.

Ex: 8-bit µP, ROM, RAM.

④ VLSI: more than 10,000 gates/chip.

(or)

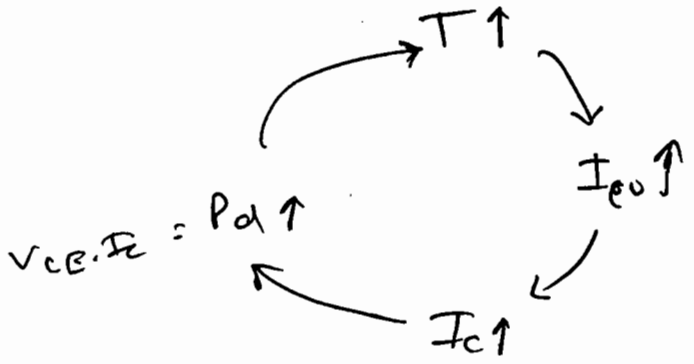
1 million Transistor/chip.

Ex: 16-bit µP, 32-bit µP.

1 - FET (Field Effect Transistor)

=> Advantages of FET.

→ Unipolar
→ Low cost
→ Low noise
→ Low Power
→ Immune to radiation.
→ High i/p impedence (use in CRO, voltmeter).
→ Low offset voltage.
→ Low thermal sensitivity.



Thermal runaway.

⇒ Thermal Stability :

$$\frac{\partial P_d}{\partial T_j} < \frac{\partial P_D}{\partial T_j}$$

$$\Rightarrow V_{CE} < \frac{V_{CC}}{2}.$$

→ BJT → CCCS

$T_p \uparrow \longrightarrow I_{CO} \uparrow \longrightarrow I_C \uparrow$

Positive temperature coefficient.

→ FET → VCCS

$T \uparrow \longrightarrow I_D \downarrow$ $\quad P_D = V_{DS} \cdot I_D.$

negative temp. coefficient.

* Features of FET:

① Unipolar device because current is due to only majority carrier only.

② High input impedence.

③ Immune to Radiation.

④ Less noisy than BJT.

⑤ No offset Voltage at zero drain current.

⑥ Thermally more stable than BJT.

⑦ Simple biasing.

→ It requires less no. of fabrication, diffusion steps therefore low cost.

→ Voltage Controlled devices that is VCCS.

* Drawback:

→ Low gain Bandwidth Product.

⇒ As transistor shrinks i.e. reduction in size it becomes faster & consumes less Power.

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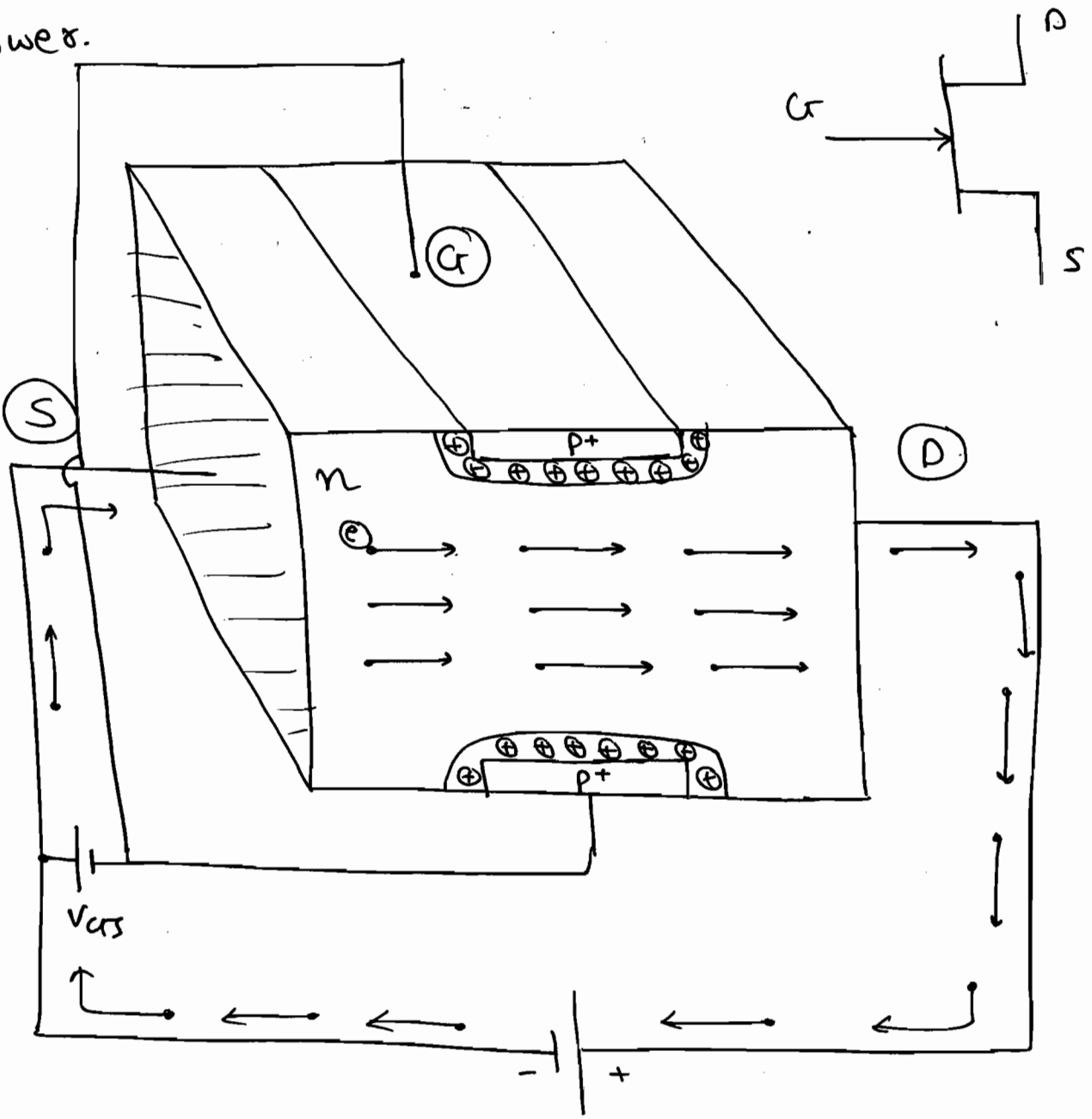
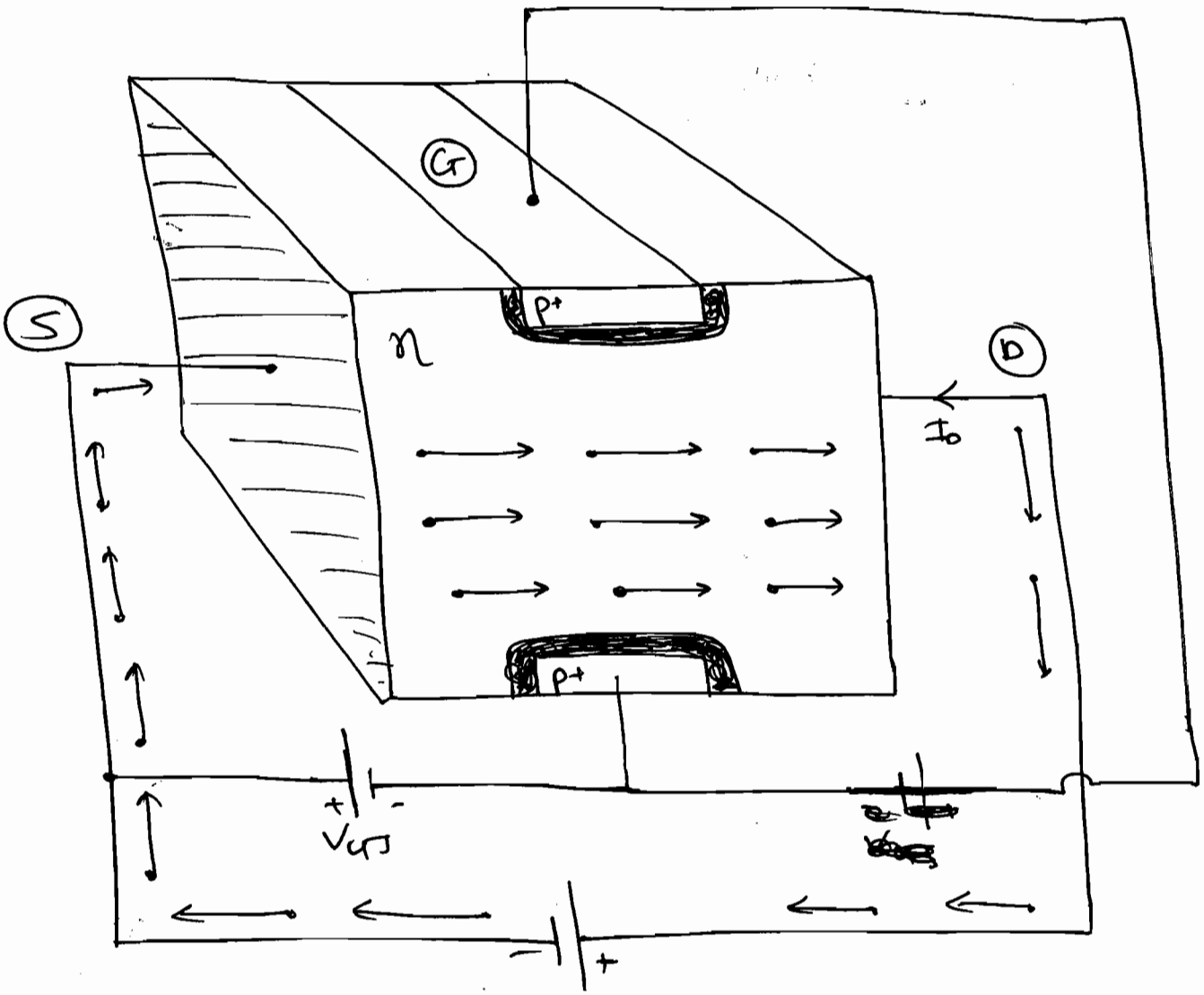


* n- Channel JFET:



$\rightarrow I = \frac{Q}{T}$ $\Rightarrow$ $I = \frac{-1.6 \times 10^{-9} N}{T}$

$= \frac{Qn}{T}$

$I = \frac{Nq}{T}$

(1) Source:

$\Rightarrow$ Source is the terminal through which majority carriers are enters into the semiconductor bar.

* **Drain:**

→ Drain is the terminal through which majority carriers are leaves from the semiconductor bar.

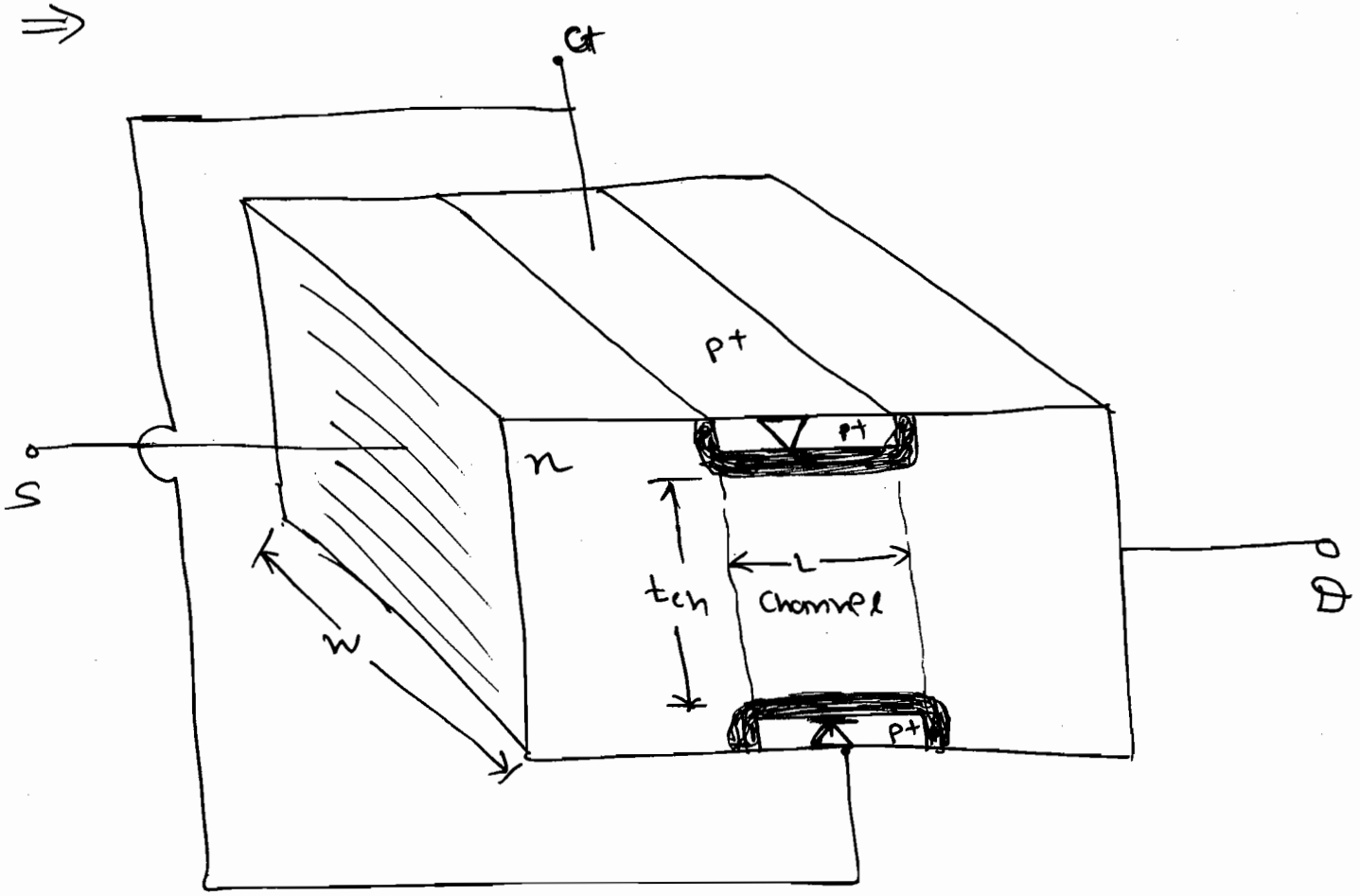
* **Gate: (or):**

⇒ Gate is the two heavily doped p^+ regions diffussed both the sides of the n-type semiconductor bar and it controlls the flow of carriers, (or) current betn source and drain.

* **Channel:**

⇒ Channel is the region betn two heavily doped p^+ gate region through which carriers moves from source to drain.

⇒



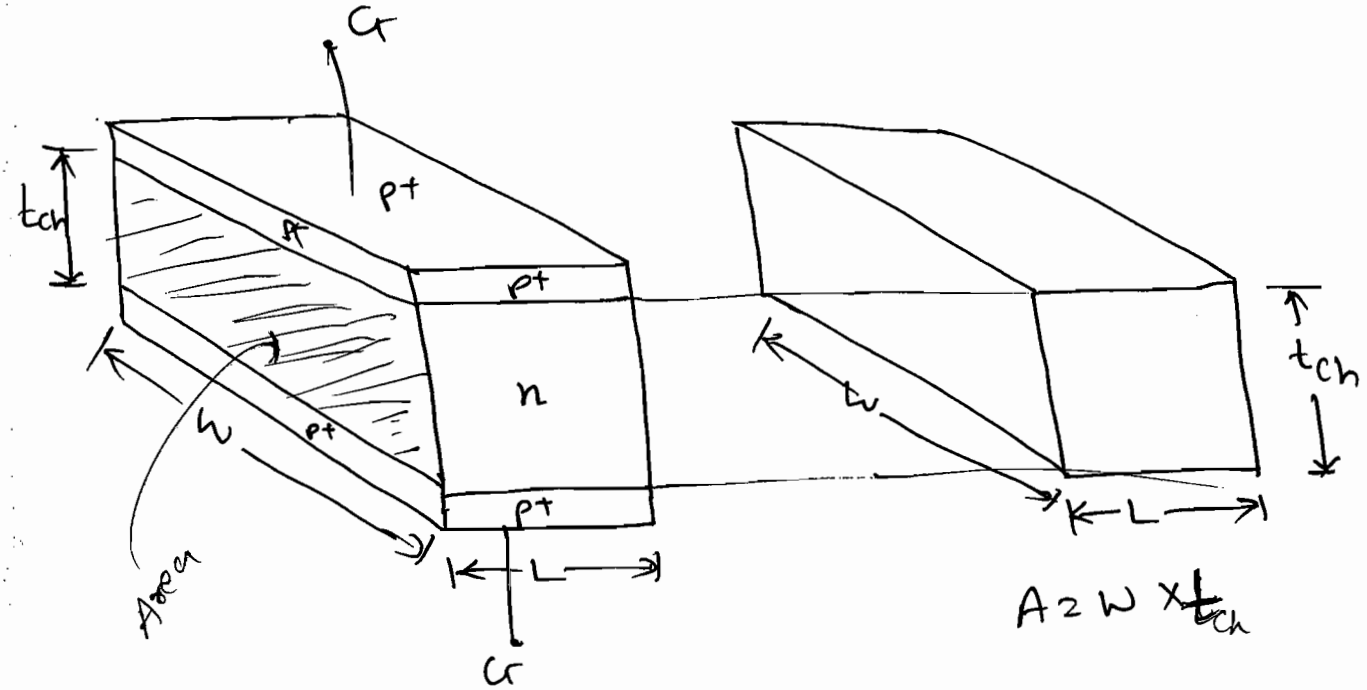
$V_j = V_o$

I_D (or) $I_{DJ} = 0$.

$$W \propto \sqrt{\frac{1}{N_A} + \frac{1}{N_D}}$$

$N_A = N_D$ $\quad N_A >> N_D$ $\quad N_D >> N_A$.

⇒ Channel Portion:



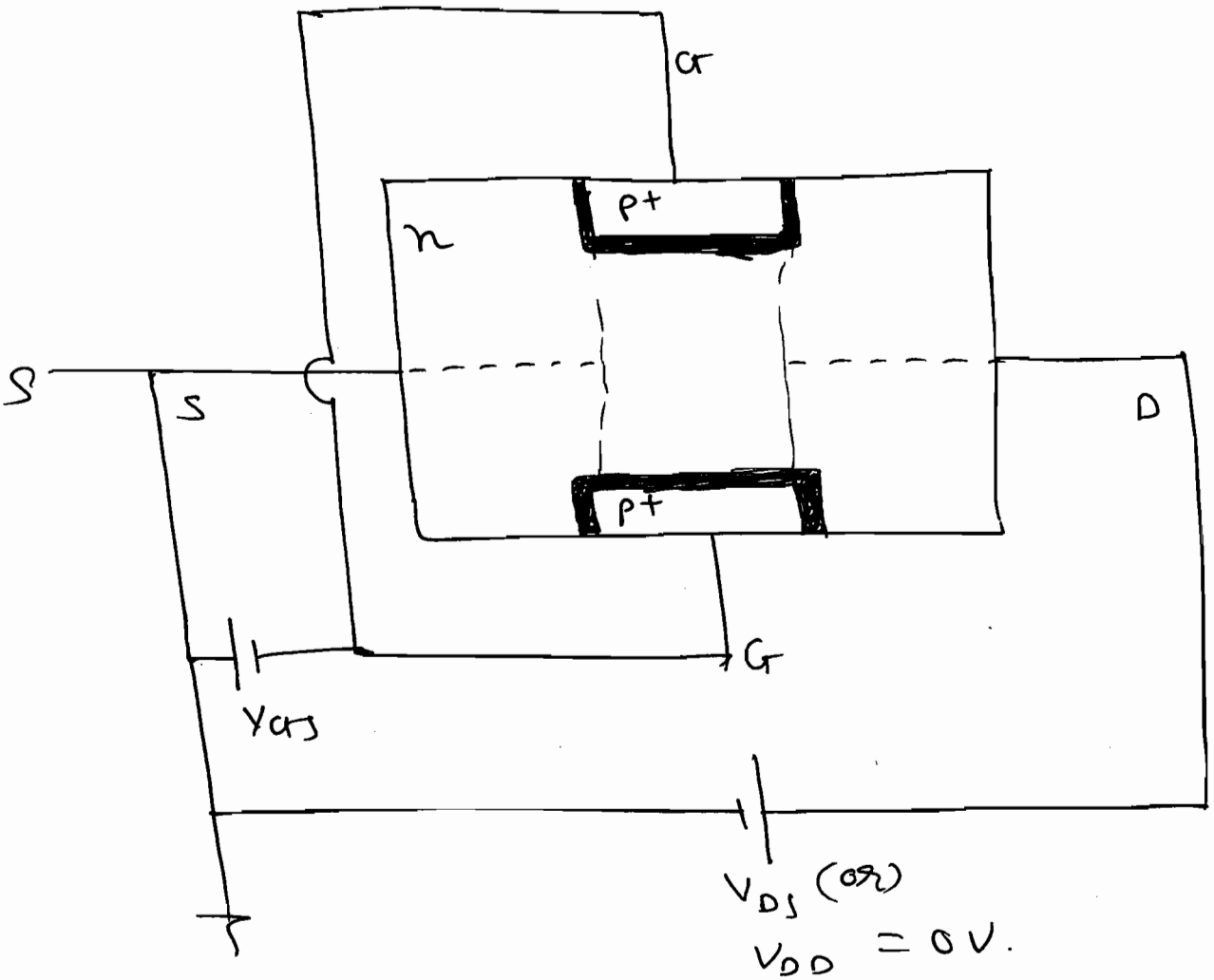
$A = W \times t_{ch}$

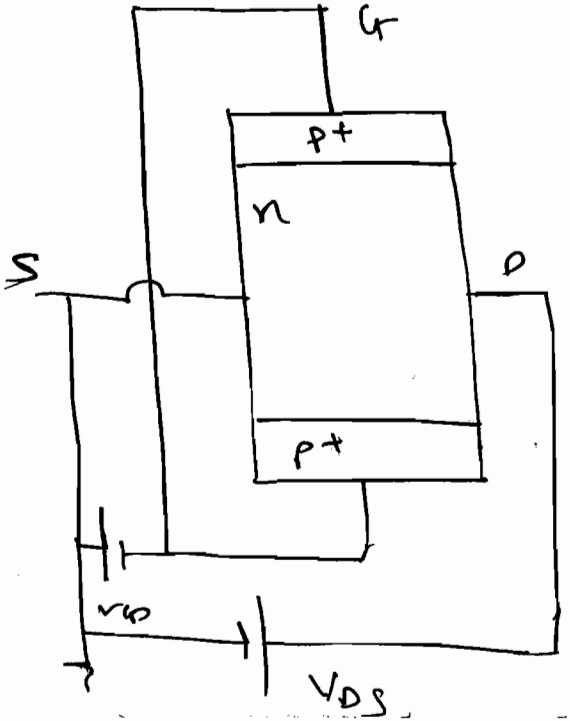
$\rightarrow \quad R = \frac{\rho L}{A} \qquad \rho_n = \frac{1}{n q \mu_n} \approx \frac{1}{N_D q \mu_n}$.

$R_{ch} = \frac{\rho L}{A}$

Let, $R_{ch} = 500\,\Omega$.

$\Rightarrow$





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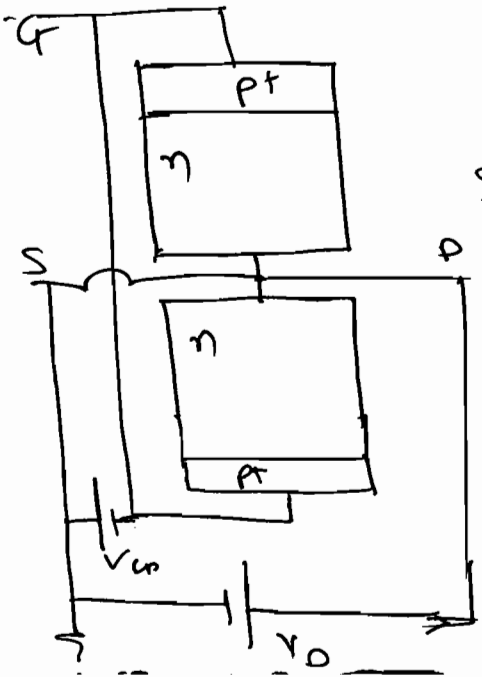

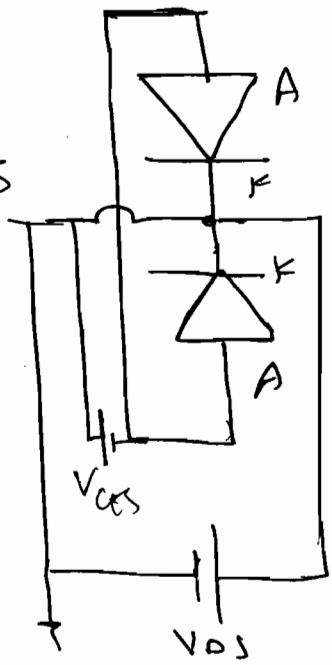

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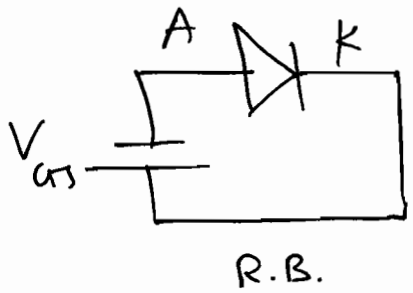

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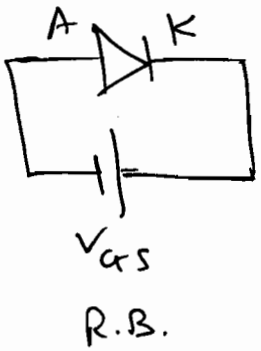
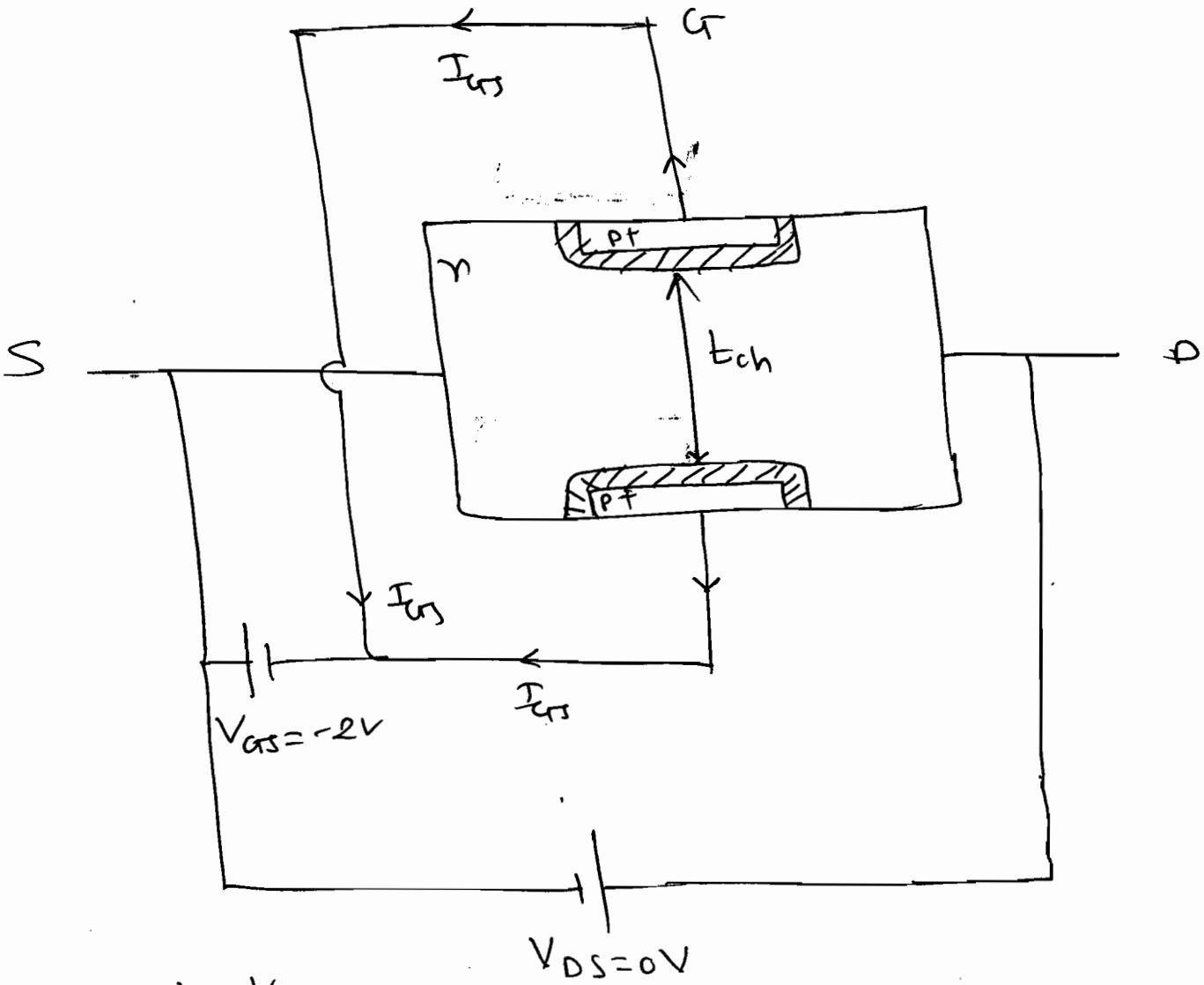


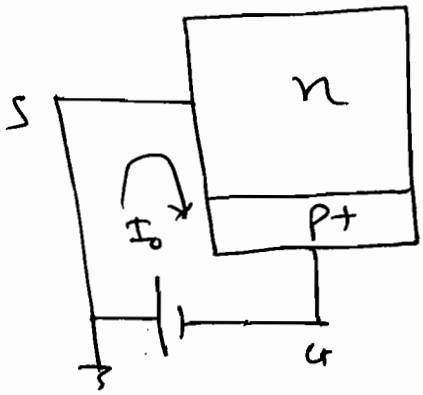
⇒ When $V_{GS} = -2V$ & $V_{DS} = 0V$



$V_j = V_0 + V_{GS}$

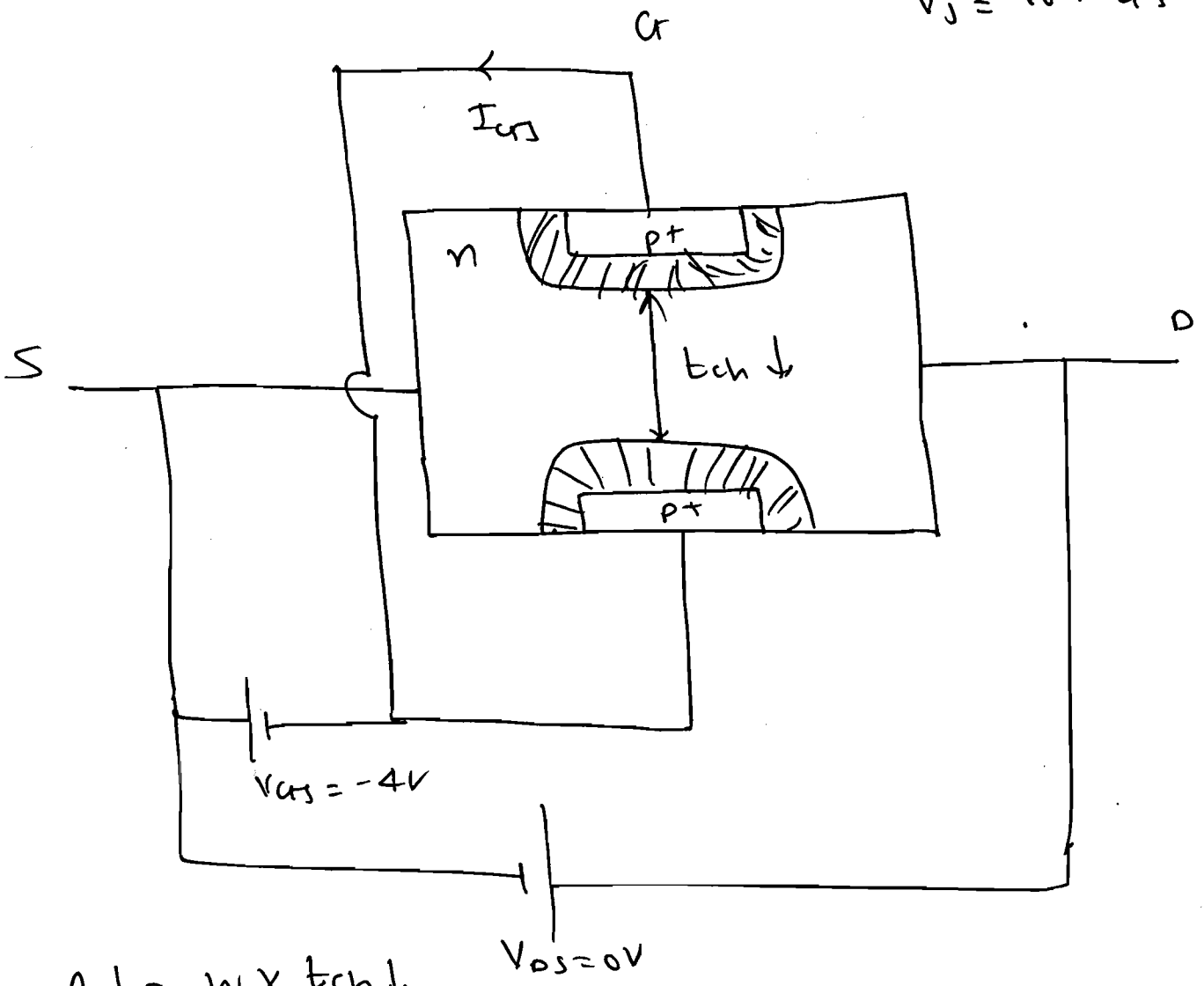
$A \downarrow = w \times t_{ch} \downarrow$

$R \uparrow = \frac{\rho L}{A \downarrow}$



$\Rightarrow$ when $V_{GS} = -4V$.

$V_j = V_0 + V_{GS}$

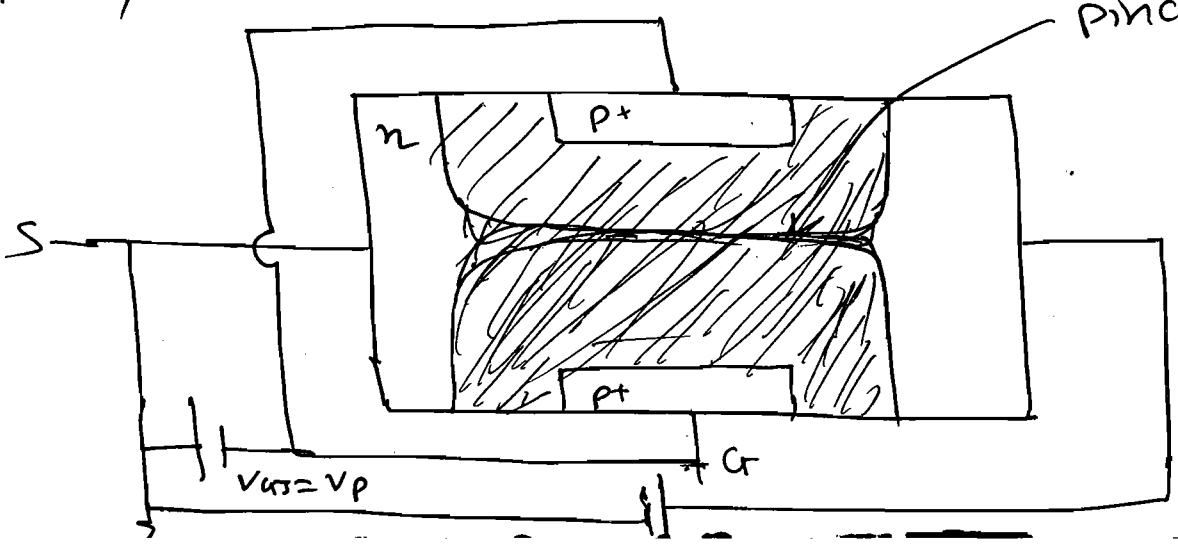


$A\downarrow = W \times t_{ch}\downarrow$

$R \updownarrow \frac{\rho L}{A\downarrow}$

$\Rightarrow$ So, this JFET can be used as Voltage ~~Regulator~~ Variable Resistor.

Now, at $V_{GS} = V_{GS(cutoff)} = V_p$.



$V_j = V_o + V_{GS}$ (cut-off).

$\Rightarrow t_{ch} = 0 \Rightarrow A = w \times t_{ch} \approx 0\ m^2$.

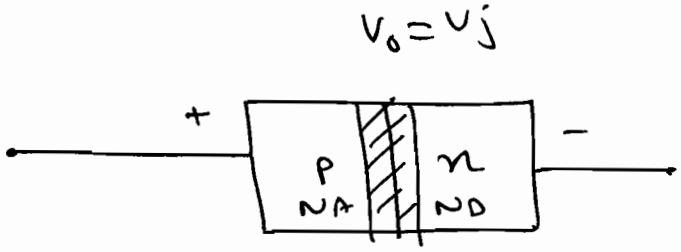
$\Rightarrow R = \frac{\rho L}{A} = \infty\ \Omega$.

$\Rightarrow R_{ch} = \infty\ \Omega$ So. open circuit.

i.e. JFET is OFF or in cut-off.

$\Rightarrow$ At particular value of V_{GS}, thickness of the channel is almost zero and no carrier is flow from source to drain end hence no current flow and JFET comes into cut-off. This condition is called pinch-off. and it ranges from -9V to -25V.

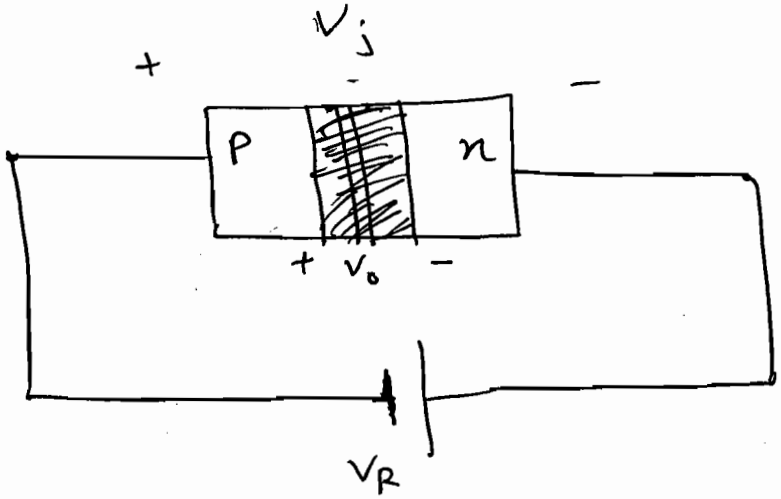
$\Rightarrow$ <u>O.C.</u>



$V_j = V_o$

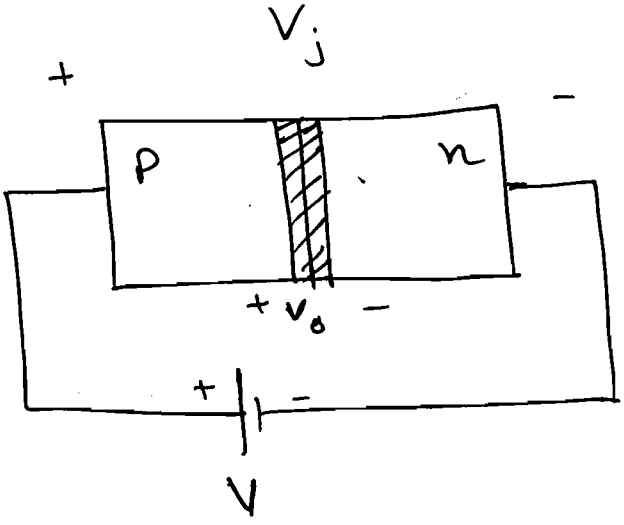
$\therefore$

$\Rightarrow$ <u>R.B</u>



$V_j = V_0 + V_R$.

⇒ F.B.



∴ By KVL, $V - V_j - V_0 = 0$.

$\therefore V_j = V - V_0$.

$V_j = V_0 - V_F$.

⇒ $\boxed{V_{GS(cut\text{-}off)} = V_{GS(off)} = V_p}$.

⇒ Condition for pinch-off:

$\therefore \boxed{V_{DS} = V_{GS} - V_p}$.

$\therefore 0 = V_{GS} - V_p \Rightarrow \boxed{V_{GS} = V_p} = -10V$.

⇒ $I_{GSS} \rightarrow nA$

I_{GSS} : Reverse Saturation Current

: Depend on temp.

: Inc by 7 % /°C.

: Double / 10°C.

I_{GSS} at T_1 (given)

I_{GSS} at T_2 = ?

$\therefore$

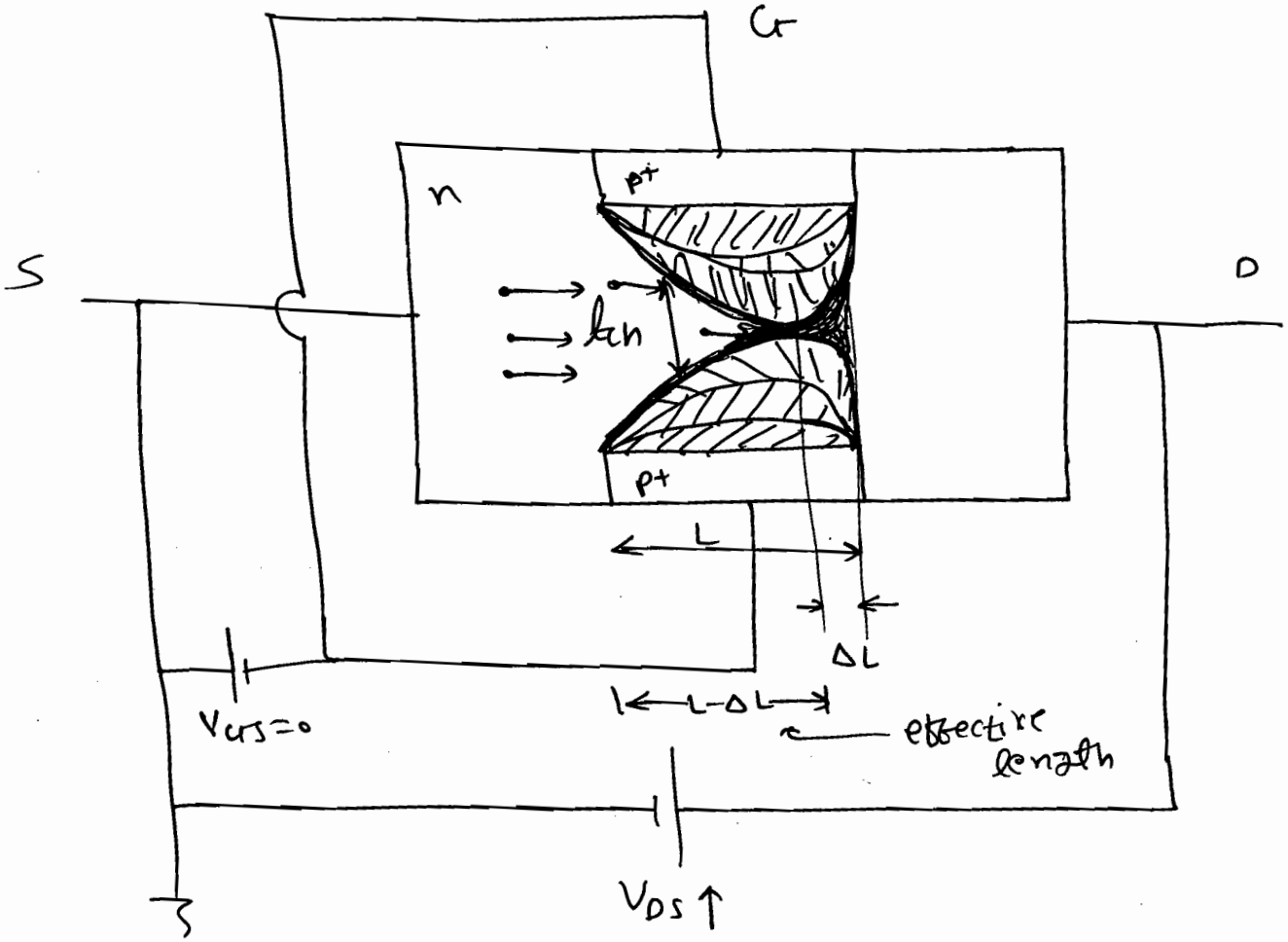
$I_{GSS}(T_2) = \uparrow$

$\Rightarrow$

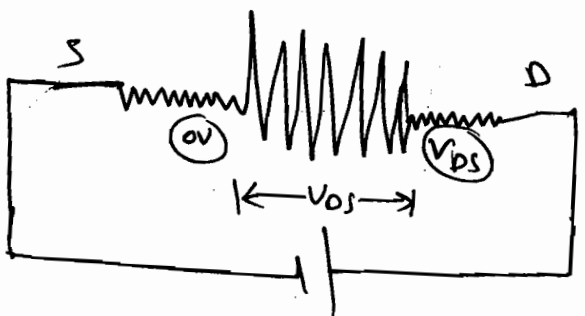
$$I_{GSS}(T_2) = 2^{\left(\frac{T_2 - T_1}{10}\right)} \cdot I_{GSS}(T_1).$$

$$I_{O2} = 2^{\left(\frac{T_2 - T_1}{10}\right)} \cdot I_{O1}(T_1).$$

Case- ii Now, $V_{GS} = 0$,

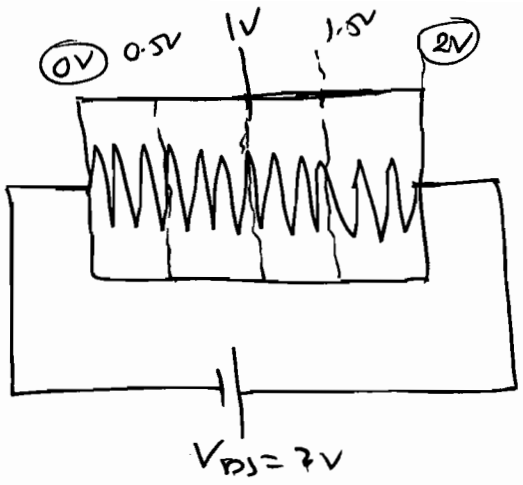


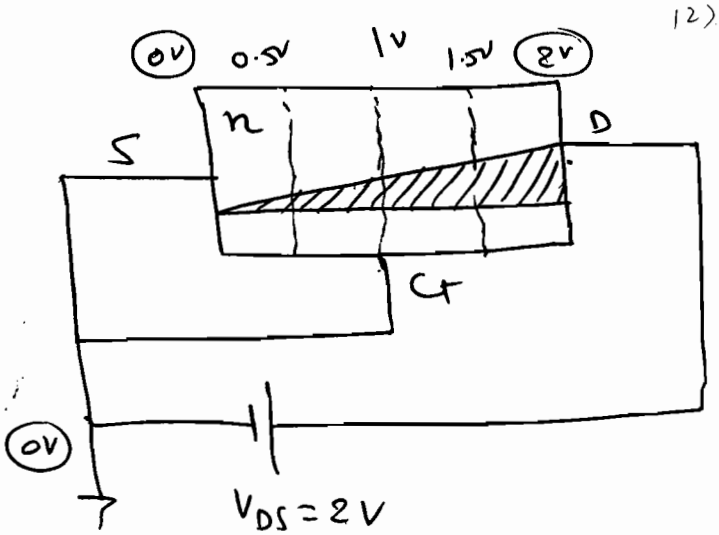
$\Rightarrow$ Resistance across the channel:



When we move from source to Drain channel Resistor is increased.

⇒



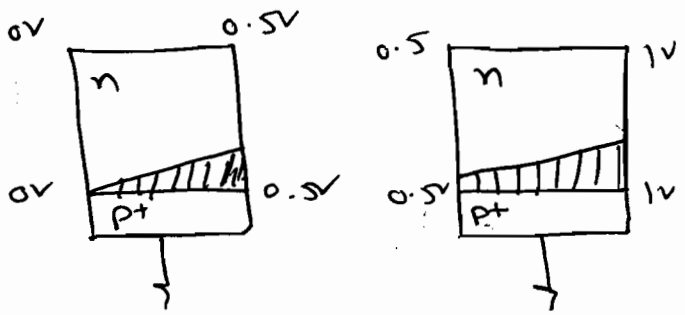


⇒ $E \uparrow = \frac{V_{DS}}{L} \uparrow$

$v \propto E$

⇒ $v_{DS} \propto E$

⇒ $I_{DS} \propto V_{DS}$.



* Condition for pinch-off:

⇒ $\boxed{V_{DS} = V_{GS} - V_P.}$

$\therefore V_{DS} = 0 - V_P$

$V_{DS} = -V_P = -(-10) = 10V.$

⇒ $E = \frac{\Delta V_{DS}}{\Delta L}$.

⇒ At ΔL portion E is constant.

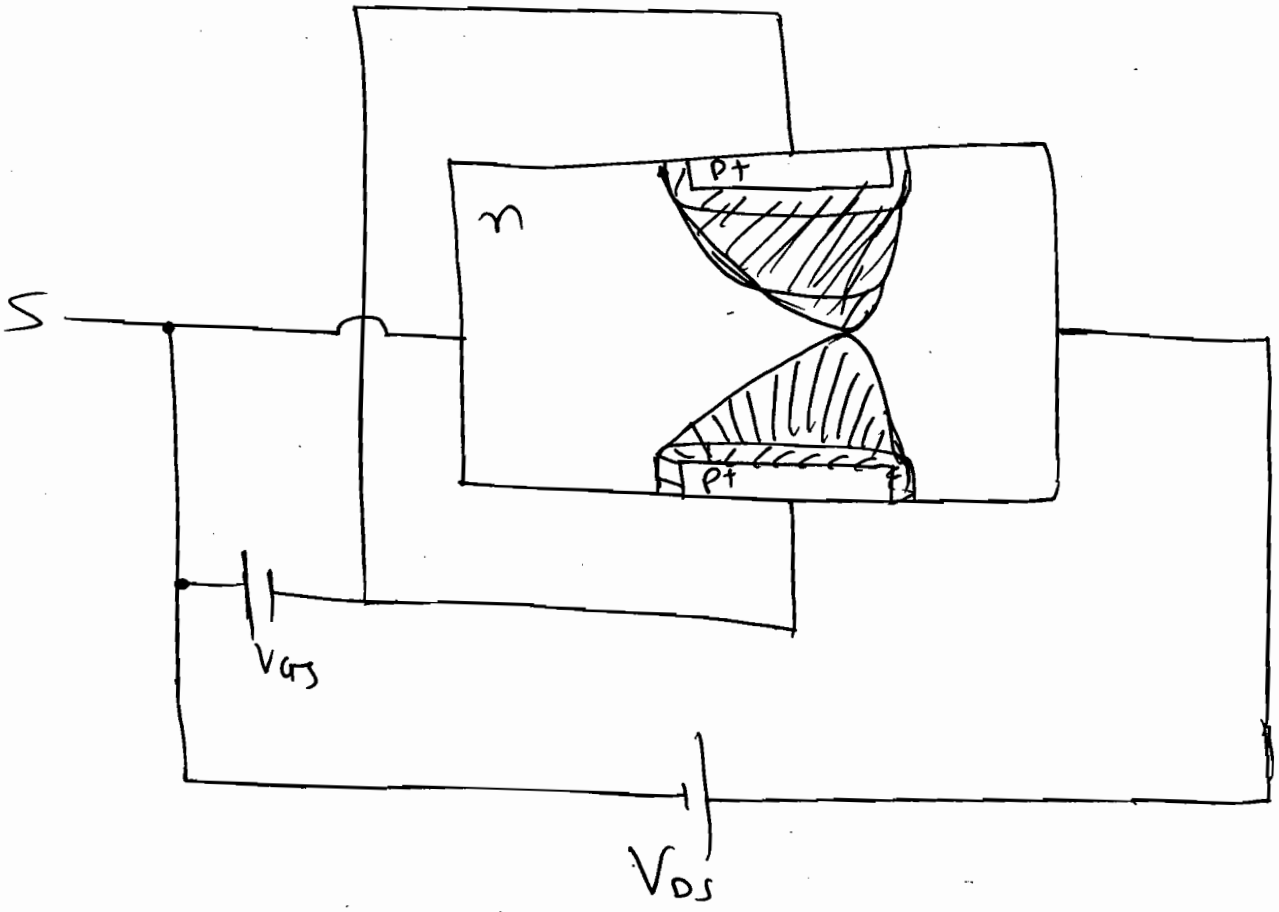
⇒ I_D (or) $I_{DS} = I_S$.

⇒ $\boxed{V_j = V_0 + V_{GS} + V_{DS}.}$

Note: In BJT we decide region of operation based on biasing of BE and CB junction. In JFET we will decide the region of operation based on the I_D current. In Sat' region

I_D remains Constant.

⇒



$$V_j = V_0 + V_{GS} + V_{DS}.$$

⇒ $V_{DS} = V_{GS} - V_P.$

$V_{GS} - V_P = -2V - (-18V) = 8V.$

if $V_{DS} = 8V$

$\Rightarrow V_{DS} = V_{GS} - V_P$

if $V_{DS} = 7V$

$\Rightarrow V_{DS} < V_{GS} - V_P.$ ⇒ operate in linear region.

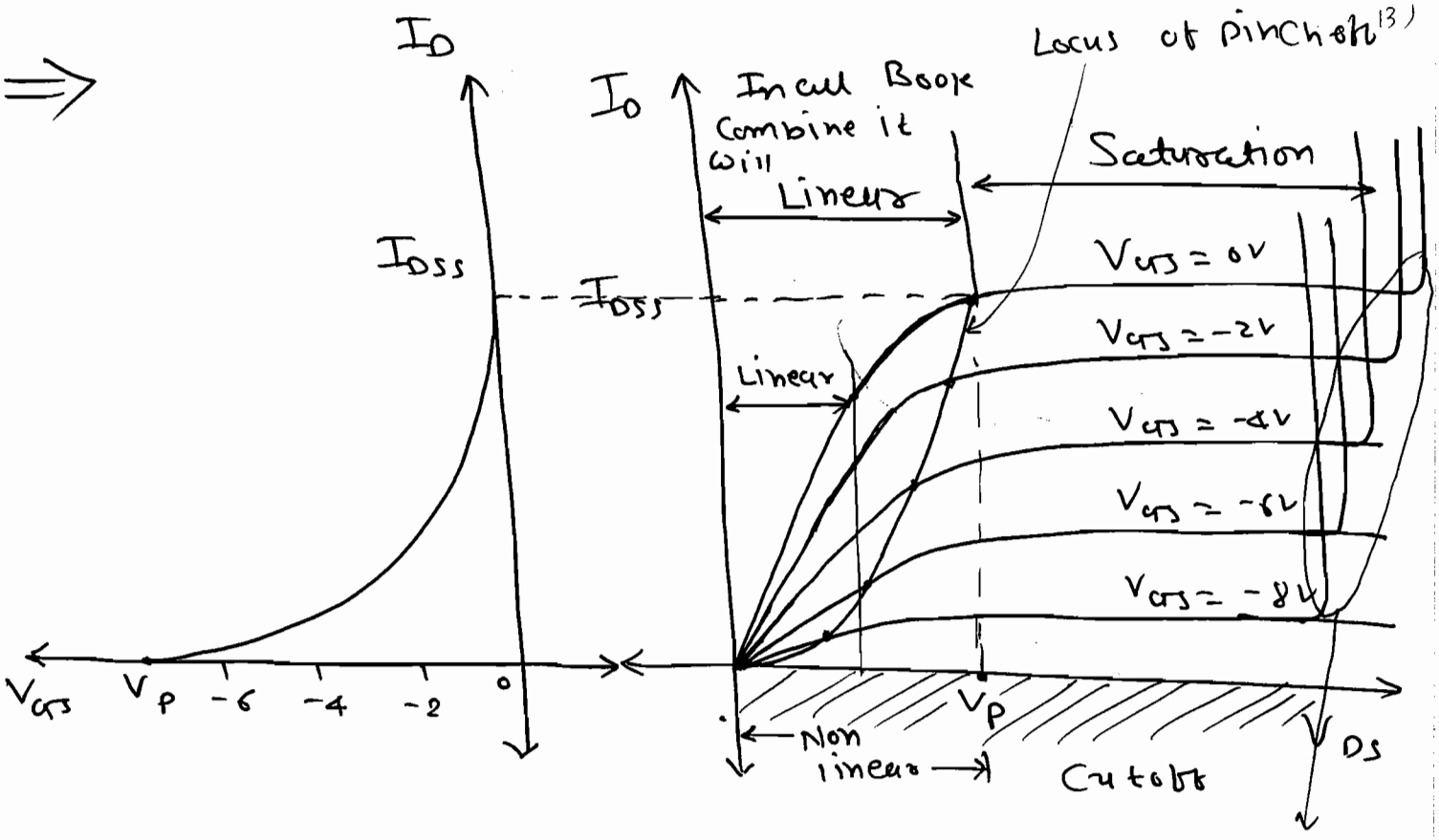
if $V_{DS} = 10V$

$\Rightarrow V_{DS} > V_{GS} - V_P$ ⇒ operate in sat. region..

$V_P = -10V$, $V_{GS} = -10$ } $V_{GS} = V_P$

$V_P = -10V$, $V_{GS} = -12$ } $V_{GS} < V_P$

} $V_{GS} \leq V_P$ ⇒ cut-off.



(Transfer Characteristics)

(Drain Characterestics)

⇒ To find the region of operation V_{GS}, V_{DS} & V_p should be known.

→ if $\boxed{V_{GS} \leq V_p \rightarrow \text{Cut-off}}$

→ $V_p < V_{GS} < 0$.

Calculate $V_{GS} - V_p$.

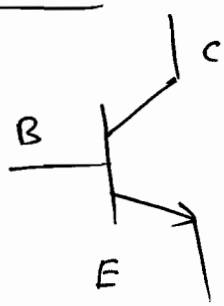
• if $V_{DS} < V_{GS} - V_p$ = linear
• if $V_{DS} > V_{GS} - V_p$ = Saturation.

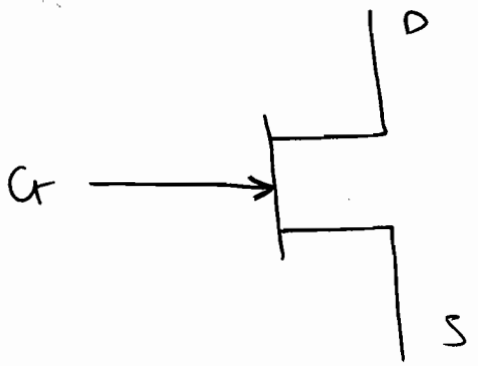
⇒ BV_{DS} = Drain to Source Breakdown voltage.

* Symbol:

Same concept as in RJT

⇒ BJT:





Direction of arrow decided Based on emitter current.

For npn it leaves and pnp it enters to the Base.

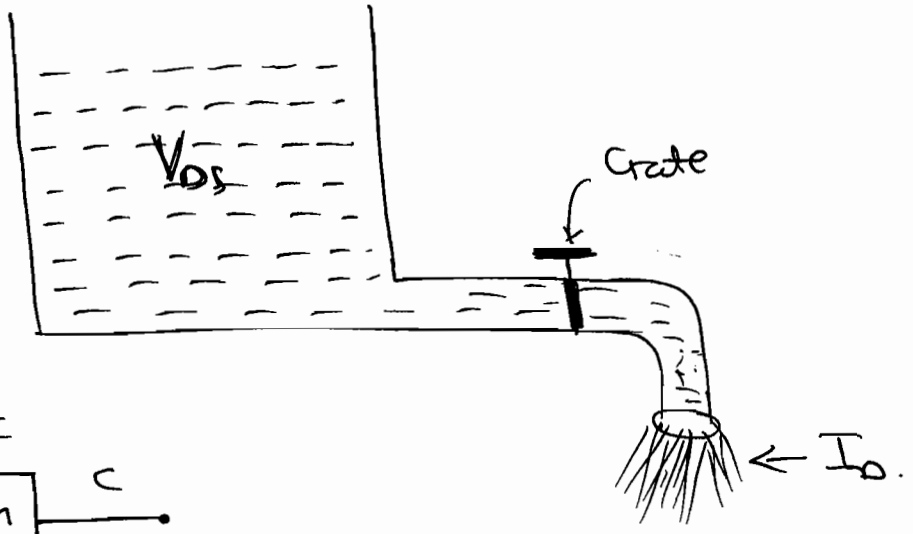
→ At $V_{GS}=0 \Rightarrow I_D = I_{DSS}$

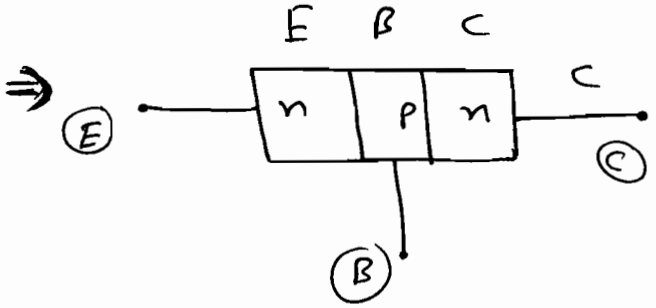
→ $I_D \leq I_{DSS}$

→ At $V_{GS}=0$

$I_S = I_D = I_{DSS}$.

⇒





⇒ BJT is not a ~~uni~~ bilateral device. It is a unilateral device. because if we change polarity of supply the current will not same.

because in BJT Carrier Concentration is not same in C & E. In BJT Collector is collector

Emitter is Emitter.

⇒ where as in JFET Drain and Source can be interchanged.

* Important points to be remember in n-Channel JFET.

⇒ n- Channel JFET operates with -ve gate to source voltage. i.e. -ve V_{GS} values.

⇒ Gate to Source Voltage and pinch- off Voltages are -ve for n-channel JFET.

⇒ n- JFET operates in depletion mode for -ve V_{GS} values.

⇒ JFET operates always in depletion mode.

⇒ JFET operates with reversed biased gate junction.

⇒ $V_{GS(cut-off)}$ Voltage is the value of the V_{GS} at which both the gate depletion regions comes close and the thickness of the channel becomes zero and also drain current $I_D = 0$. ($V_{DS} = 0$).

⇒ pinch- off Voltage is the minimum value of V_{DS} at which drain current

becomes constant. ($V_{GS}=0$).

⇒ The relation bet^n $V_{GS(cut-off)}$ voltage and V_P is

$$\boxed{V_{GS(cut-off)} = V_{GS(off)} = V_P.}$$

⇒ In n-channel JFET as V_{GS} decreases (i.e. increasing in -ve direction) pinch-off voltages happens for lower values of V_{DS}.

⇒ Condition for pinch-off (or) Saturation is

$$\boxed{V_{DS} = V_{GS} - V_P}$$

(+ve) (-ve) (-ve)

⇒ In n-JFET as V_{GS} increases avalanch break-down happens due to avalanch effect for lower values of V_{DS}.

⇒ JFET operates in linear, saturation and cut-off region.

⇒ Linear region is the region which is left side to the pinch-off locus.

⇒ Sat. region is the region Right side to the pinch-off locus.

⇒ Cut-off region is the region below $V_{GS}=V_P$.

⇒ JFET can be used as Amplifier in a Sat. region and it can be used as a switch in a linear and cut-off regions.

⇒ JFET can be used as Voltage Variable Resistor in linear region and it can be operate as a Current source in saturation region.

⇒ Linear region is also called as 'Ohmic region' (or) triode region.

⇒ Transfer char. of a JFET gives pinch-off Voltage (V_p), I_{DSS} and trans conductance (g_m).

⇒ For $V_{GS} \leq V_p$ n-channel JFET operates in cut-off region and its drain current $I_D = 0A$.

⇒ For $V_p < V_{GS} < 0$ & $V_{DS} < V_{GS} - V_p$ it operates in linear region and its drain current

$$\therefore \boxed{I_D = \frac{2 I_{DSS}}{V_p^2}\left[(V_{GS} - V_p)V_{DS} - \frac{1}{2}V_{DS}^2\right].}$$

(-ve, -ve, +ve)

⇒ For $V_p < V_{GS} < 0$ and $V_{DS} \geq V_{GS} - V_p$ it operates in sat region. and its drain current

$$\boxed{I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_p}\right]^2}$$

(-ve, -ve)

Note:

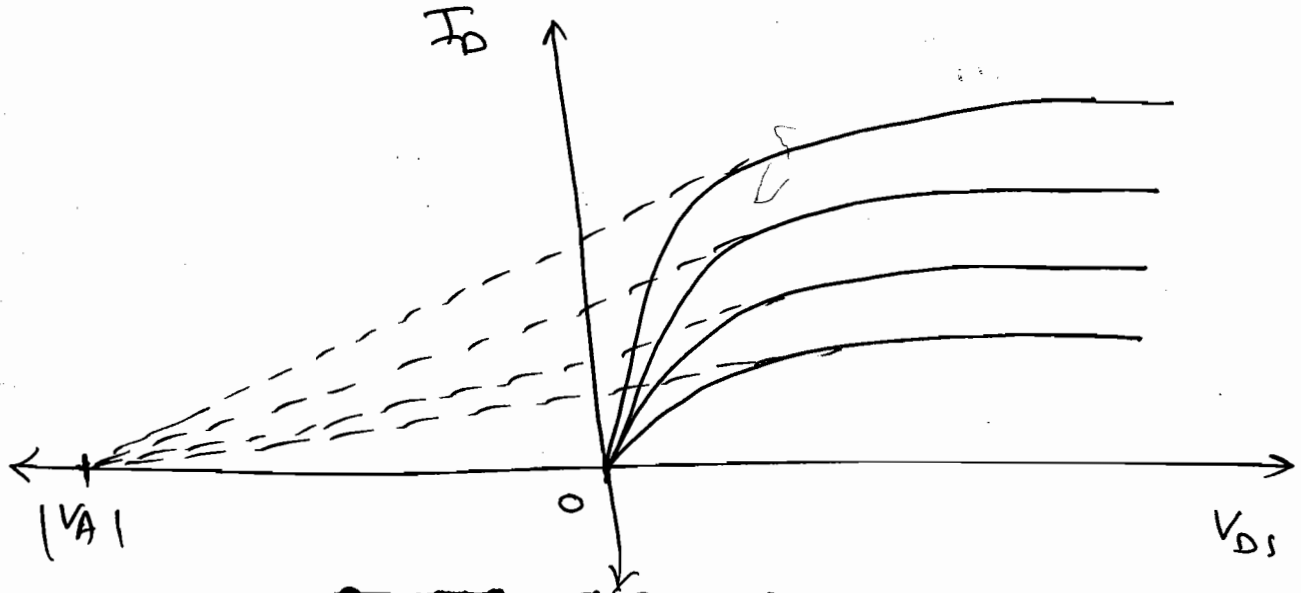
⇒ JFET is a Symmetrical device therefore Source and Drain terminal can be interchanged.

* Channel Length Modulation:

⇒ In Saturation region as drain to Source voltage increases the effective length of the channel is decreases i.e. as V_{DS} varies, the length of the Channel is also varies. i.e. called Channel length Modulation. Due to Channel length Modulation Drain current increases as

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2 (1 + \lambda V_{DS}).$$

where, λ is channel length modulation parameter. $\lambda = \frac{1}{V_A}$, V_A = early Voltage.



* Drain Resistance (or) o/p resistance:

⇒ It is the Resistance offered by the JFET in the Sat. region.

⇒ It is the reciprocal of the slope of Drain characteristics in the ~~str~~ saturation region.

⇒ $$r_d \text{ (or) } r_o = \frac{1}{\left.\frac{\Delta I_D}{\Delta V_{DS}}\right|_{V_{GS}}} = \left.\frac{dV_{DS}}{dI_D}\right|_{V_{GS}}.$$

⇒ Drain Resistance (or) o/p Resistance are also called Ac resistance (or) Small signal resistance.

⇒ $$r_d \text{ (or) } R_o = \frac{1}{\lambda I_D} = \frac{V_A}{I_D} \quad \left(\because \frac{1}{\lambda} = V_A\right).$$

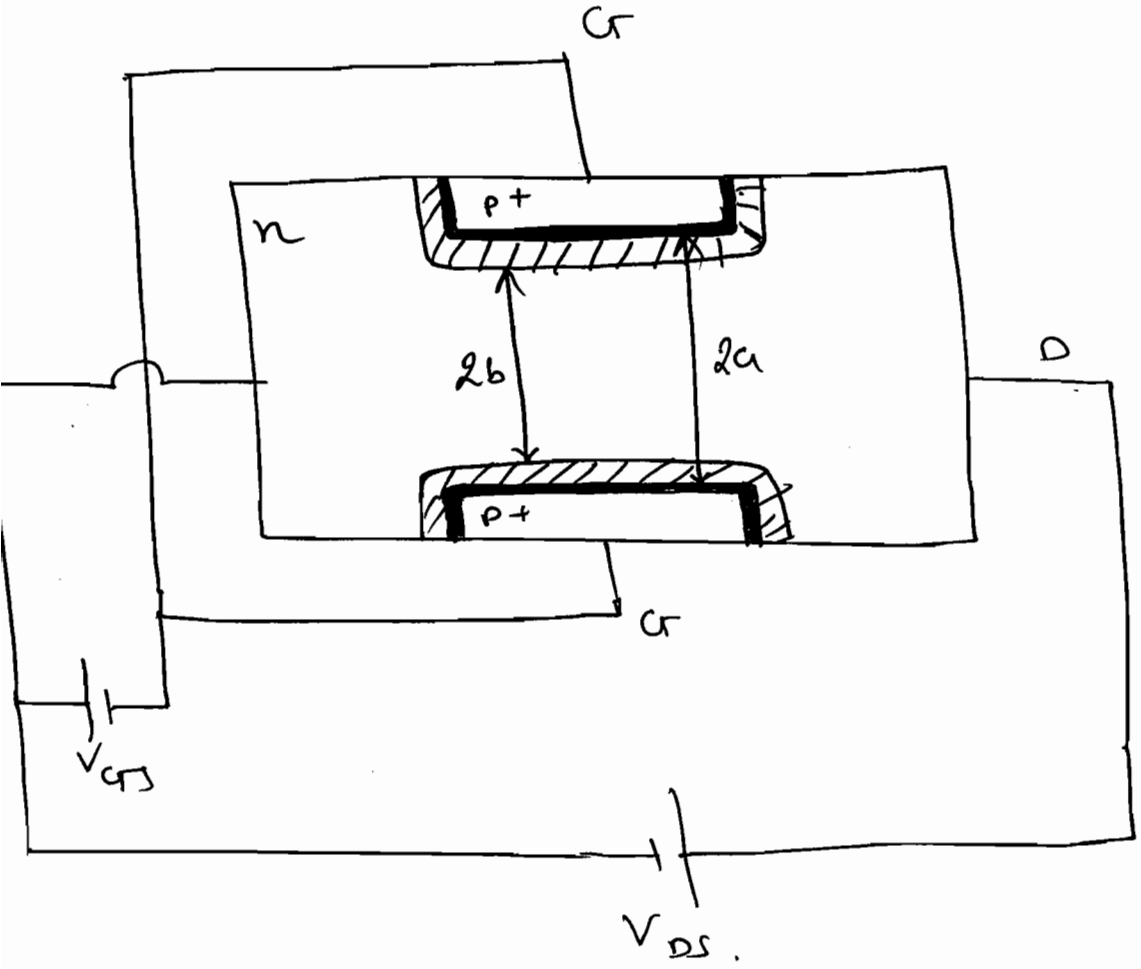
→ It ranges from 50 kΩ to 100kΩ.

* Trans Conductance (g_m):

⇒ Trans Conductance is also called as mutual Conductance (or) figure of merit.

⇒ It gives how effectively JFET converts Voltage changes at the input to the corresponding current changes at the o/p in the saturation region.

$$g_m = \left.\frac{\Delta I_D}{\Delta V_{GS}}\right|_{V_{DS}} = \left.\frac{dI_D}{dV_{GS}}\right|_{V_{DS}}.$$



a = half-channel thickness (or) width at $V_{GS} = 0$ V.

b = half-channel thickness (or) width at a given V_{GS}.

Pinch-off Voltage of a n-JFET:

$$V_p = \frac{eN_D}{2\epsilon} \cdot a^2 \Rightarrow V_p = -ve$$

$e = -1.6 \times 10^{-19}$ C.

ϵ = Permitivity of Si

$\epsilon = \epsilon_0 \epsilon_r$.

$\epsilon_r = 11.7 \approx 12$.

$\epsilon_0 = 8.85 \times 10^{-12}$ F/m.

$\epsilon_0 = 8.85 \times 10^{-14}$ F/cm.

a = half-channel thickness at $V_{GS} = 0$.

⇒ Pinch-off Voltage of a P-JFET:

→ $$V_p = \frac{e N_A}{2\epsilon} \cdot a^2$$

$e = 1.6 \times 10^{-19}$ C = Charge of hole

N_A = acceptor concentrate.

$\boxed{V_p = +ve}$

* Relation B/w V_{GS} & V_p:

⇒ $$\boxed{V_{GS} = \left[1 - b/a\right]^2 \cdot V_p}$$

⇒ $$\boxed{b = a\left[1 - \sqrt{\frac{V_{GS}}{V_p}}\right]}$$

Ex-1 An n-channel JFET has Channel thickness of 10μm at $V_{GS} = 0V$. Calculate its channel thickness at $V_{GS} = -5V$. Assume $V_p = -10V$.

Soln: Here, $2a = 10\mu m$ & $2b = ?$

$V_p = -10V$

$$\therefore 2b = a\left[1 - \sqrt{\frac{V_{GS}}{V_p}}\right]$$

$$\therefore 2b = 2a\left[1 - \sqrt{\frac{V_{GS}}{V_p}}\right]$$

$$\therefore 2b = 10\mu\left[1 - \sqrt{\frac{-5}{-10}}\right]$$

$$\Rightarrow 2b = 10\mu\left[1 - \frac{1}{\sqrt{2}}\right]$$

$$\boxed{2b = 2.93\ \mu m}$$

= thickness of channel at $V_{GS} = -5V$.

* Drain ON Resistance (or) ON Resistance:

$\Rightarrow r_{dON}$ (or) $r_{ds(ON)}$ (or) $r_{(ON)}$

$\Rightarrow$ It is the resistance offered by the JFET in linear region. for small value of V_{DS}.

$\Rightarrow$ It is the reciprocal of the slope of the drain characteristics in the linear region. for small value of V_{DS}.

$$\Rightarrow R_{ON} = \left.\frac{1}{\frac{\Delta I_D}{\Delta V_{DS}}}\right|_{V_{GS}} = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS}}$$

$$= \left.\frac{dV_{DS}}{dI_D}\right|_{V_{GS}}$$

$$r_{d(ON)} = \frac{L}{2aW N_D \mu_n q \left[1 - \sqrt{\frac{V_{GS}}{V_P}}\right]}.$$

$r_{d(ON)}$ = Drain ON resistance at a given V_{GS}.

$\Rightarrow$ At $V_{GS} = 0V$

$$\Rightarrow r_{d_0(ON)} = \left.\frac{L}{2aW N_D \mu_n q}\right|_{V_{GS}=0}.$$

$$\therefore r_{d(ON)} = \frac{r_{d_0(ON)}}{\left(1 - \sqrt{\frac{V_{GS}}{V_P}}\right)}.$$

$\Rightarrow r_{d(ON)} > r_{d_0(ON)}$. it ranges from 100 Ω to 100 kΩ.

* Temperature effect:

⇒ Case-(i) : V_p

V_p : dependent on Temp.

: Inc by 2.2 mV / °C.

$T\uparrow \rightarrow V_p\uparrow \rightarrow I_D\uparrow$

PTC

PTC: +ve Temp. Coefficient.

(OR)

$T\uparrow \rightarrow t_{ch}\uparrow \rightarrow R_{ch}\downarrow \rightarrow I_D\uparrow$

PTC

$T\uparrow \rightarrow I_D\downarrow$

NTC

⇒ Case-(ii): μ

$\mu \propto \frac{1}{T^m}$ (or) $\mu \propto T^{-m}$

Si : m = 2.5 for ele. → $\mu_n \propto \frac{1}{T^{2.5}}$

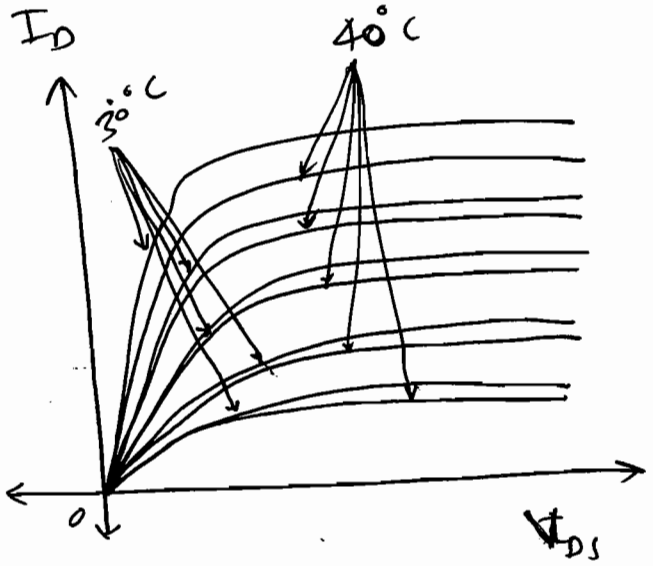
= 2.7 for holes. → $\mu_n \propto \frac{1}{T^{2.7}}$.

Ge : m = 1.66 for ele.

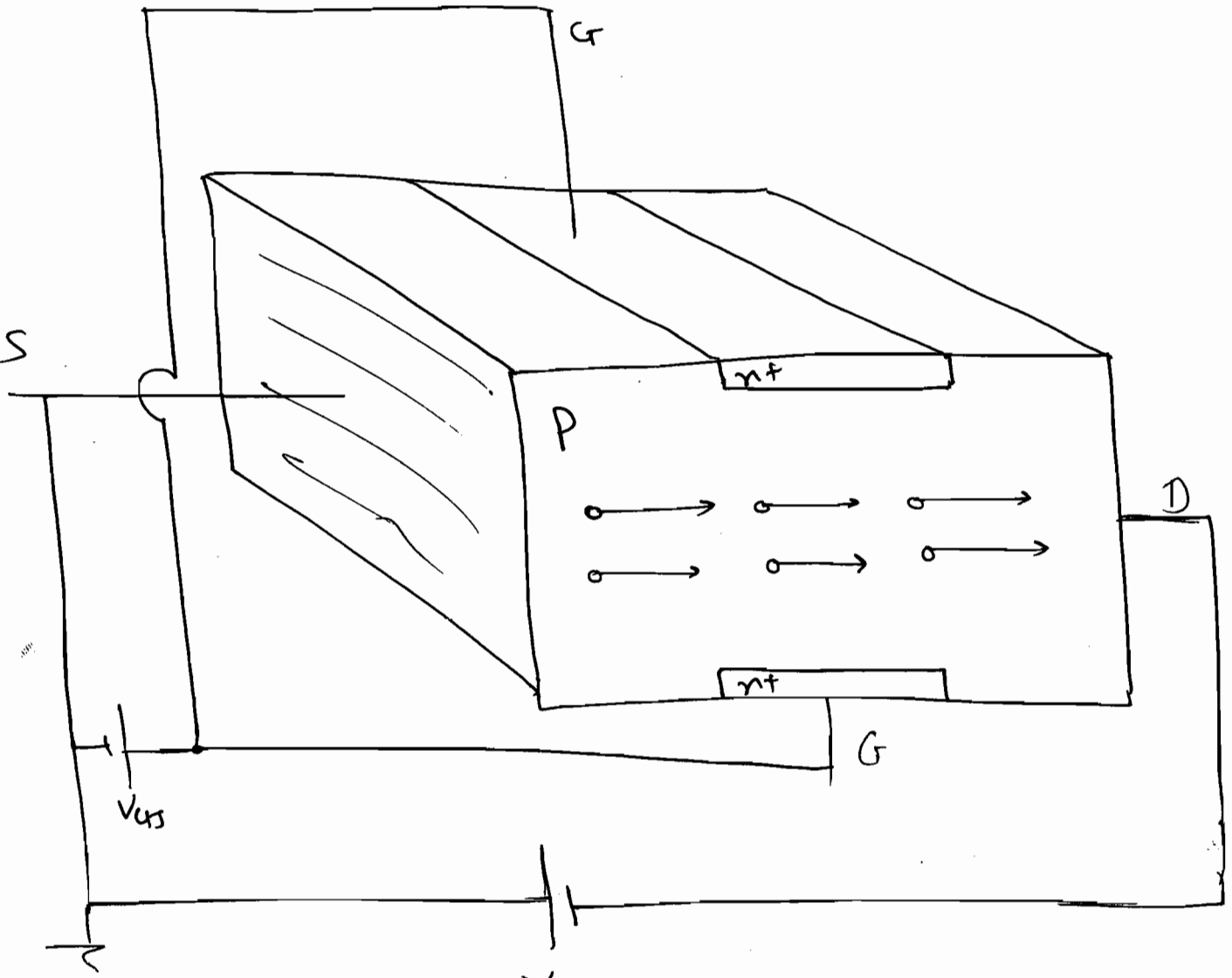
= 2.33 for holes.

$T\uparrow \rightarrow \mu\downarrow \rightarrow I_D\downarrow$.

NTC



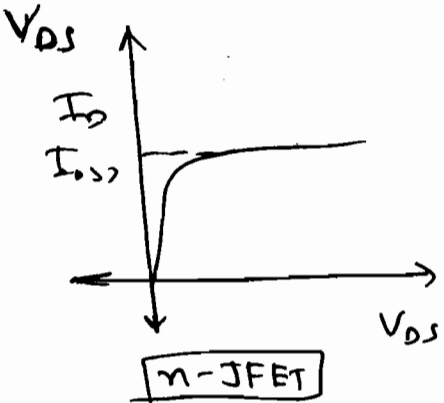
* P- Channel JFET:

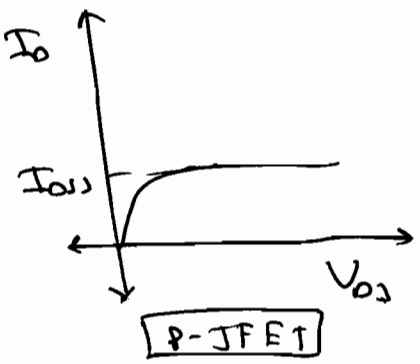


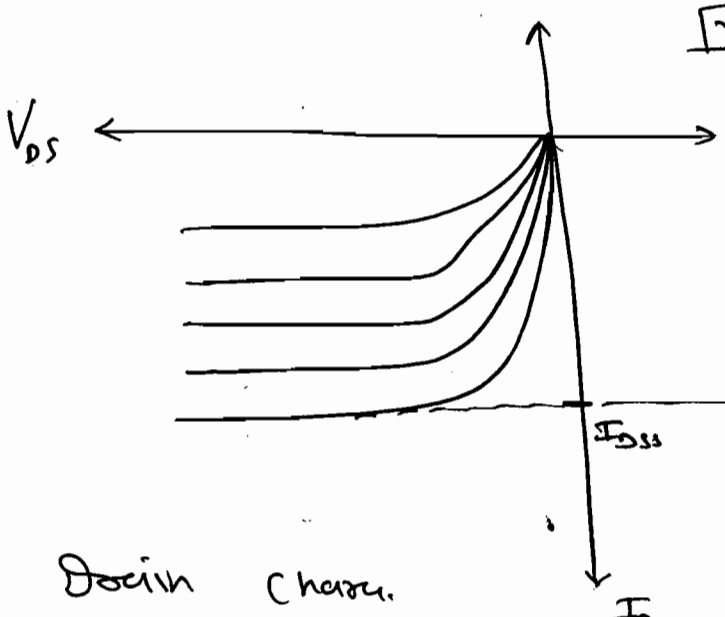
V_{DS}: +ve

V_{GS}: +ve

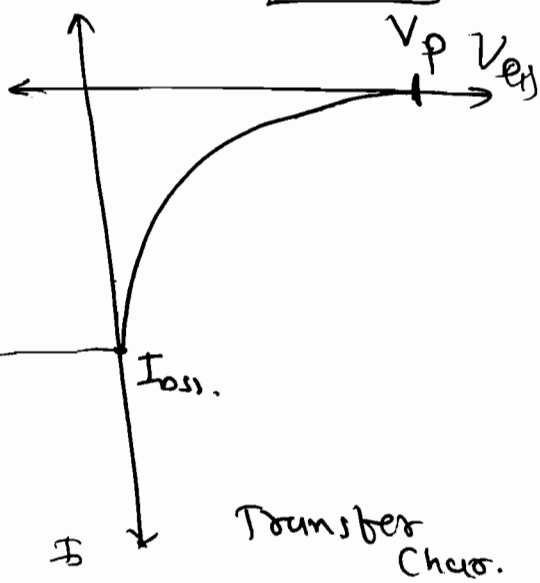
V_P: +ve







Drain Charc.



Transfer Charc.

$\Rightarrow V_{DS} = V_{GS} - V_P$.

$-ve \quad +ve \quad +ve$.

let, $V_P = +10V$, $V_{GS} = 10V$ $\Big\}$ $V_{GS} = V_P = 10V$

$V_P = 10V$, $V_{GS} = 12V$ $\Big\}$ $V_{GS} > V_P$ $\Big\}$ V_{GS}

$0 < V_{GS} < V_P \rightarrow$ Linear (or) Sat.

$V_{GS} - V_P = 2 - 10V = -8V$

if $V_{DS} = -8V$

if $V_{DS} = -7V$

$V_{DS} > V_{GS} - V_P \Rightarrow$ linear region.

for $V_{DS} < V_{GS} - V_P \Rightarrow$ Sat. region.

* Imp Points to be Remember for P-JFET:

⇒ P-channel JFET operates with +ve gate Voltages i.e. +ve V_{GS} values.

⇒ Gate to source Voltage (V_{GS}) and pinch-off Voltages (V_P) are +ve for P-JFET.

⇒ P-JFET operates in depletion mode for +ve V_{GS} values.

⇒ In P-JFET as V_{GS} increases pinch-off happens for higher values of V_{DS}.

⇒ Condition for pinch-off (or) Sat.

$$V_{DS} = V_{GS} - V_P$$

(+ve, +ve, -ve)

⇒ In p-channel JFET as V_{GS} increases Avalanch - Breakdown happens due to avalanch effect for higher values of V_{DS}.

⇒ For $V_{GS} \geq V_P$ p-channel JFET operates in cut-off region and its drain current $I_D = 0$.

⇒ For $0 < V_{GS} < V_P$ & $V_{DS} > V_{GS} - V_P$ it operates in linear region and its drain current,

$$I_D = 2\frac{I_{DSS}}{V_P^2}\left[(V_{GS} - V_P)V_{DS} - \frac{1}{2}V_{DS}^2\right].$$

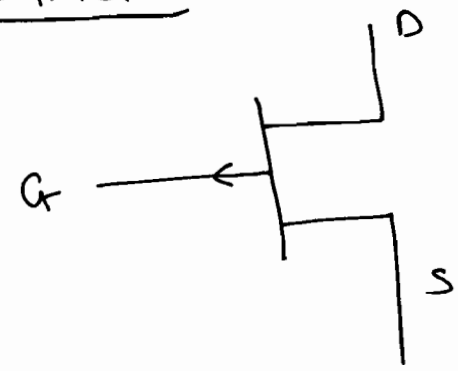
(+ve, +ve, -ve)

⇒ For $0 < V_{GS} < V_P$ & $V_{DS} < V_{GS} - V_P$, it operates in ~~linear~~ saturation region and its drain current,

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

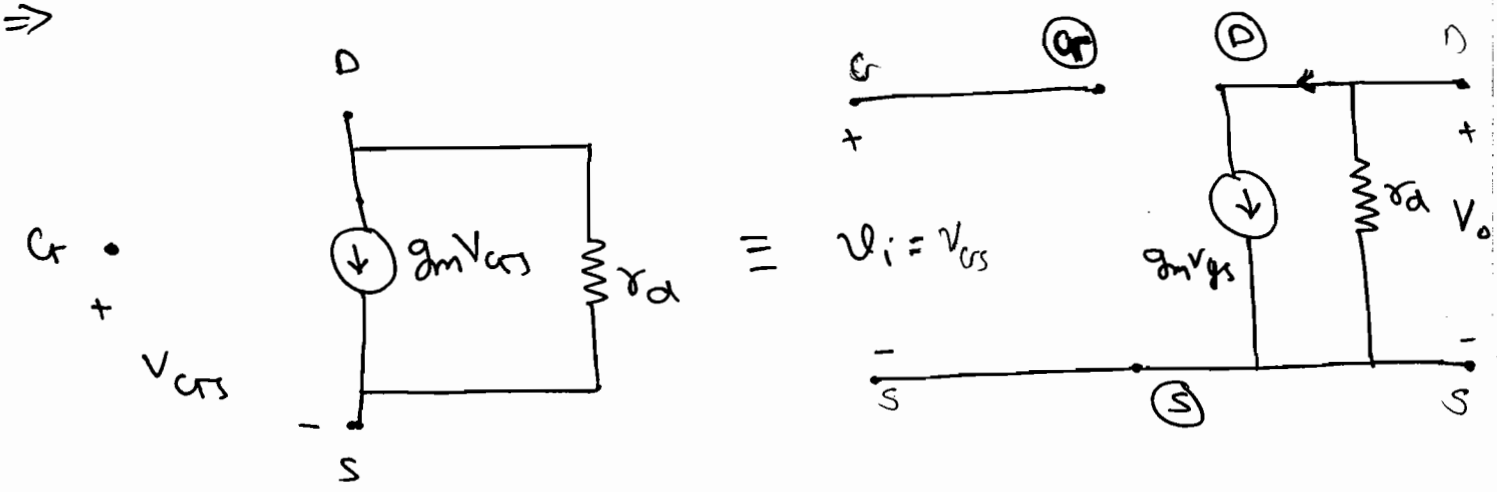
(+ve, +ve)

* Symbol :

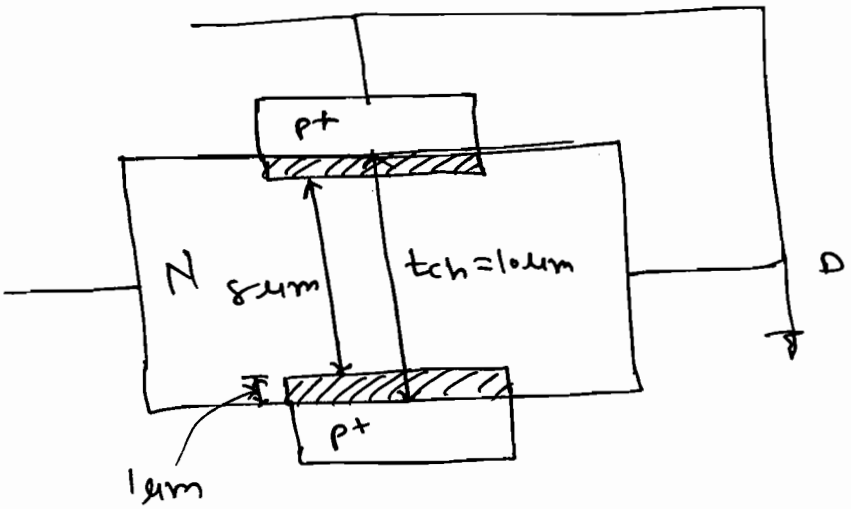


* Small signal equivalent ckt (or) AC equivalent ckt.

⇒



(a)



$V_{bi} = -1V$.

fixed Channel resistance when $V_{GS} = 0V$.

$R_{ch} = 600\ \Omega$ when $t_{ch} = 10\mu m$.

$R_{ch} = ?$ when $t_{ch} = 8\mu m$.

Soln:

$$R_{ch_1} = \frac{\rho L}{w \times t_{ch_1}}, \quad R_{ch_2} = \frac{\rho L}{w \times t_{ch_2}}.$$

$$\therefore \quad \frac{R_{ch_1}}{R_{ch_2}} = \frac{t_{ch_2}}{t_{ch_1}}.$$

$$\therefore \quad R_{ch_2} = \frac{t_{ch_1}}{t_{ch_2}} \times R_{ch_1}$$

$$= \frac{10}{8} \times 600$$

$$\boxed{R_{ch_2} = 750\ \Omega}$$

Q-10 The channel Resistance when $V_{GS} = -3V$.

Soln:

$$V_j = \frac{eN_D}{2\epsilon} \cdot W^2$$

$$\therefore V_j \propto W^2$$

when $V_{GS} = 0$, $V_j = V_B = -1V. = V_{bi}$

when $V_{GS} = -3$ $V_j = V_0 + V_B = -1 - 3 = -4V.$

$W = 1\mu m$ when $V_{GS} = 0.$

$$\therefore \quad \frac{V_{j1}}{V_{j2}} = \left(\frac{W_1}{W_2}\right)^2.$$

$$\therefore \quad \frac{-4}{-1} = W_2^2 = \frac{V_{j2}}{V_{j1}} \times W_1^2$$

$$\therefore \quad W_2^2 = \frac{-4}{-1} \times (1\mu m)^2.$$

$$\therefore \quad \boxed{W_2 = 2\mu m}$$

$$\therefore \quad \text{Now,} \quad t_{ch_3} = 10 - 2 - 2 = 6\mu m.$$

$$\therefore \quad \frac{R_{ch_3}}{R_{ch_1}} = \frac{t_{ch_1}}{t_{ch_3}}.$$

$$\therefore \quad R_{ch_3} = \frac{10}{6} \times 600.$$

$$\boxed{R_{ch_3} = 1000\ \Omega}$$

⇒ FET :

$T \uparrow \uparrow \longrightarrow I_D \downarrow$ $\quad P_D = V_{SD} \cdot I_D$

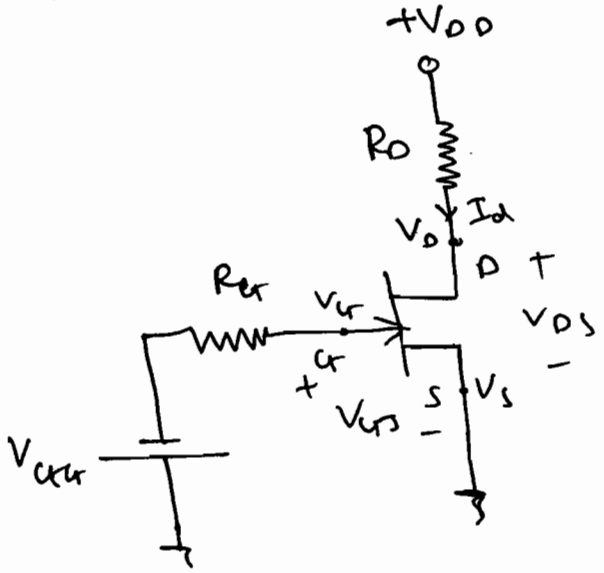
NTC

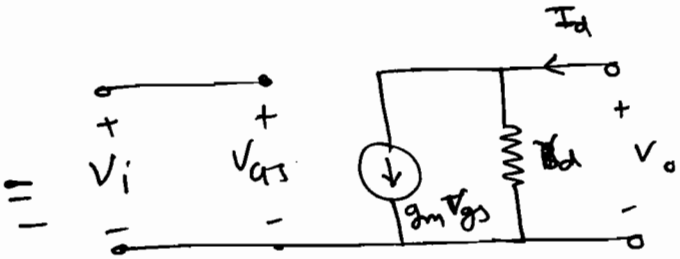
⇒ FET is very much stable than BJT as it has -ve temp. coefficient.

* Biasing techniques For JFET: [DC analysis]

① Fixed biased.
② Self biased.
③ Voltage divider biased.

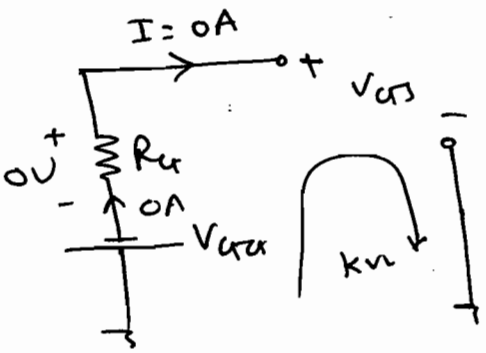
① Fixed biased :



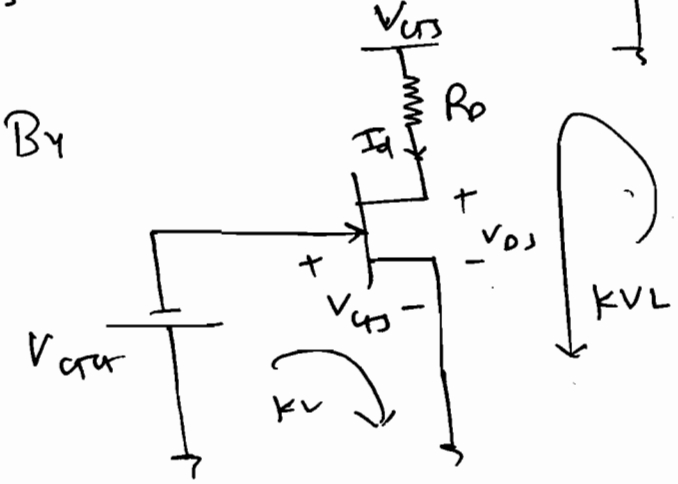


⇒ $V_{DS} = V_D - V_S$

$V_{GS} = V_G - V_S$



⇒ By



$\Rightarrow$ By KVL $\quad -V_{GG} - V_{GS} = 0.$

$$\therefore \boxed{V_{GS} = -V_{GG}}$$

$\Rightarrow$ $$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

$$\therefore \boxed{I_D = I_{DSS}\left[1 + \frac{V_{GG}}{V_P}\right]^2}$$

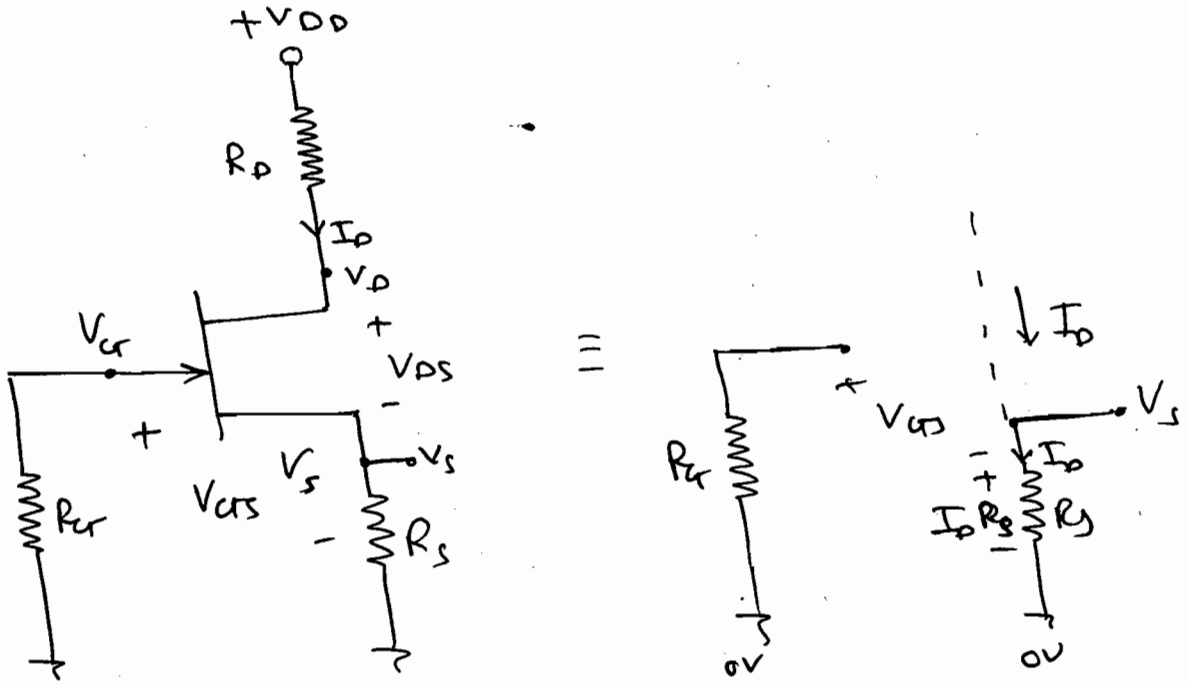
$\Rightarrow$ By KVL,

$$V_{DD} - I_D R_D - V_{DS} = 0.$$

$$\therefore \boxed{V_{DS} = V_{DD} - I_D R_D.}$$

(2) Self - biased :

$\Rightarrow$



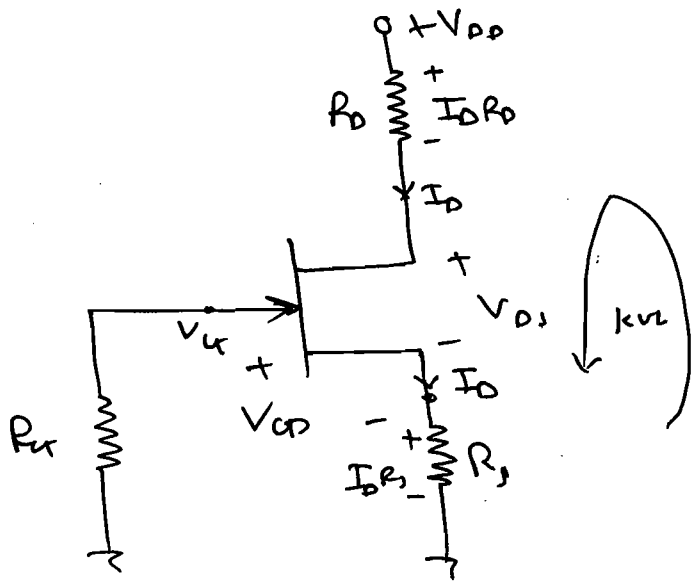
$\Rightarrow V_{GS} = V_G - V_S$

By, KVL $\quad 0 - V_{GS} - I_D R_S = 0$

$$V_{DS} = V_D - V_S.$$

$\Rightarrow$ $$\boxed{V_{GS} = -I_D R_S.}$$

$\Rightarrow$



$\Rightarrow$ By, KVL, $\quad V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0.$

$\therefore \quad V_{DS} = V_{DD} - I_D (R_D + R_S).$

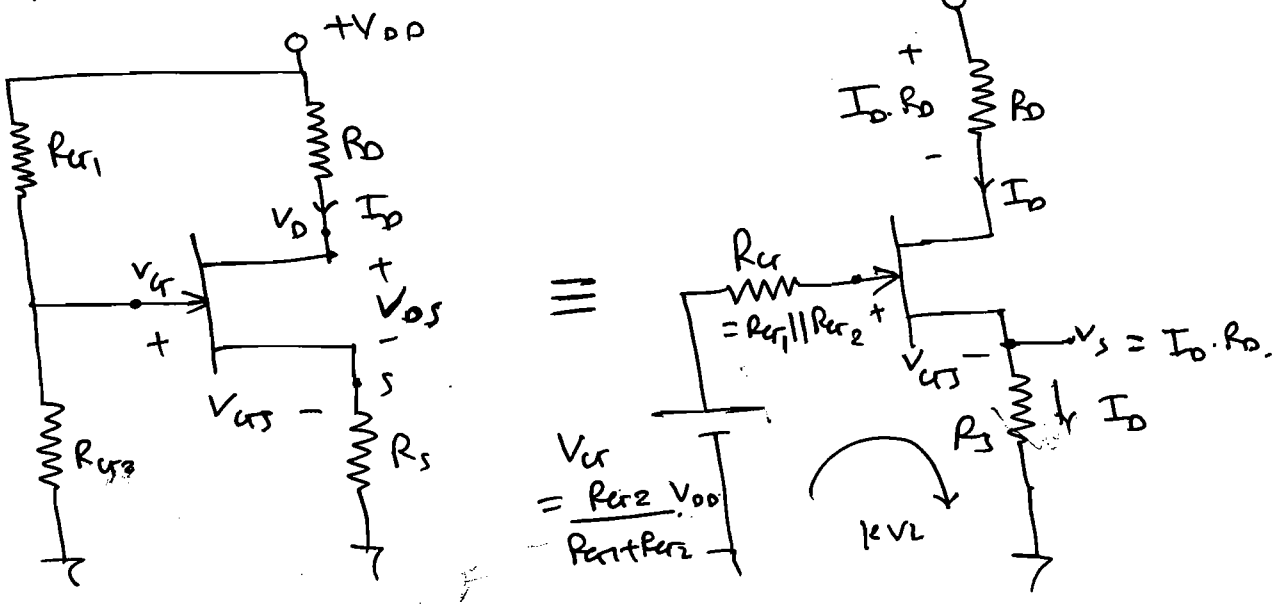
But, $\quad I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$

$V_{GS} = -I_D \cdot R_S$ $\quad \because$

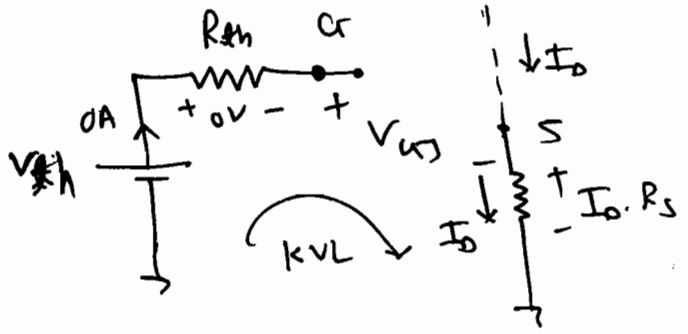
$\therefore \quad I_D = I_{DSS}\left[1 + \frac{I_D R_S}{V_P}\right]^2$ $\quad \because$

$\therefore \quad \boxed{V_{DS} = V_{DD} - I_{DSS}\left[1 + \frac{I_D R_S}{V_P}\right]^2 \cdot (R_D + R_S)}$ $\quad \because$

(3) Voltage - Divider biased:



$\Rightarrow V_{GS} = V_G - V_S$



$\Rightarrow V_G = V_{th} + 0$

$V_G = V_{th}.$

$V_G - V_{GS} - I_D.R_S = 0.$

$\therefore$

$$\therefore \boxed{V_{GS} = V_G - I_D.R_S.}$$

$$V_G = V_{th} = \frac{R_{G2}}{R_{G1}+R_{G2}} \times V_{DD}.$$

$$\Rightarrow I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2.$$

$$\therefore \boxed{I_D = I_{DSS}\left[1 - \frac{V_G - I_D.R_S}{V_P}\right]^2.}$$

$$\Rightarrow V_{DD} = I_D.R_D + V_{DS} + I_D.R_S.$$

$$\therefore \boxed{V_{DS} = V_{DD} - I_D(R_D + R_S).}$$

Now, V_{GS} should be -ve.

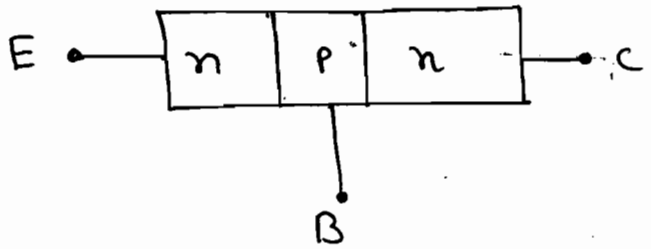
So, $I_D.R_S > V_G.$

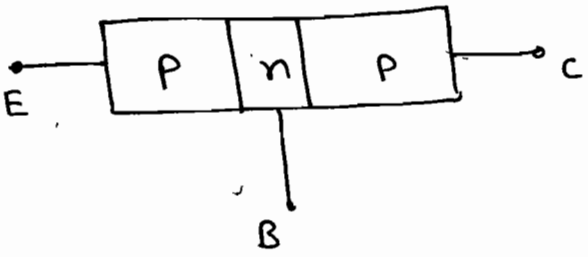
$$\frac{V_{DS} - V_{DD}}{R_D + R_S}.R_S > V_G$$

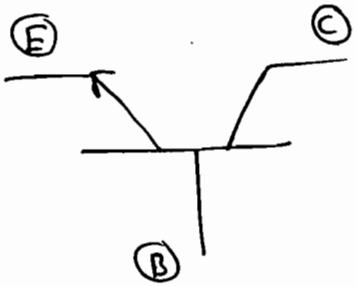
Select R_D & R_S in such a way that $I_D.R_S > V_G \Rightarrow V_{GS} = -ve.$

✡ Amplifier Analysis: (AC Analysis):

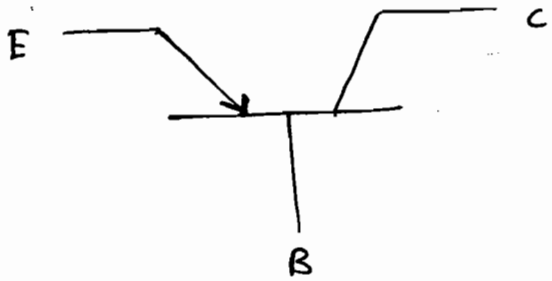
⇒







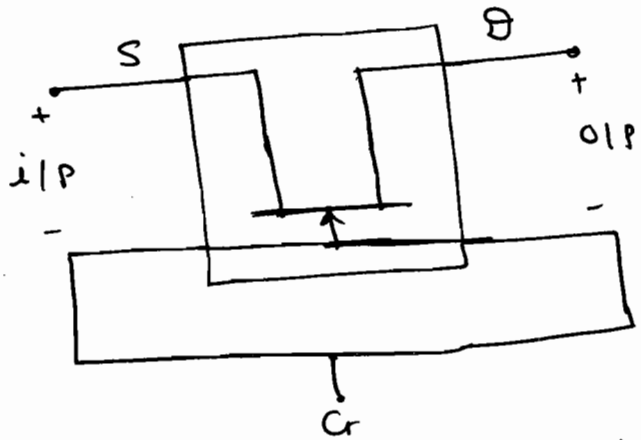
(npn)



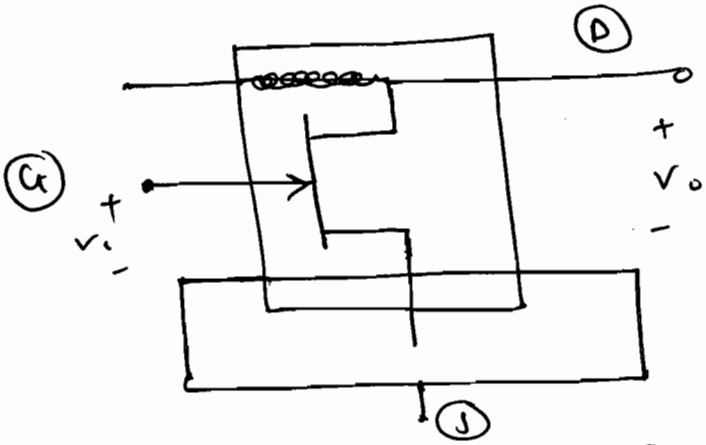
(pnp)

⇒ Configuration of JFET:

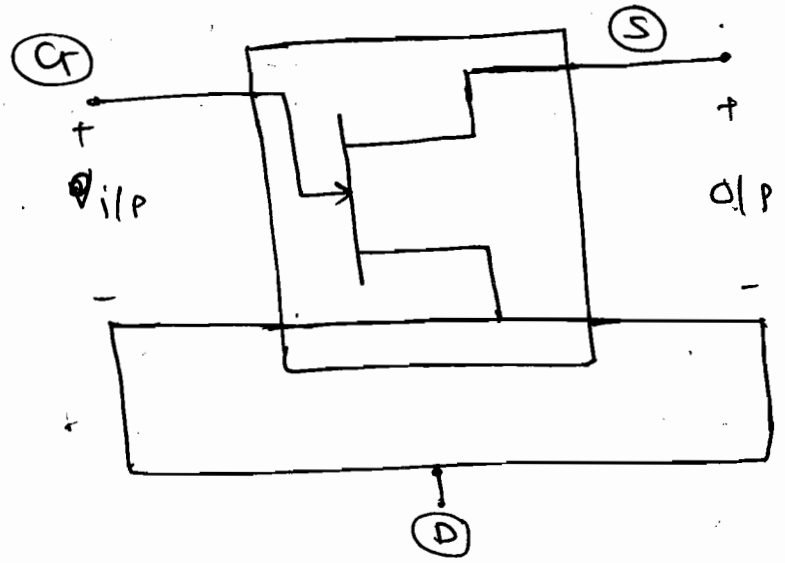
① Common gate Configuration:



② Common Source configuration:



(3) Common Drain Configuration:



(Source follower)

Note:

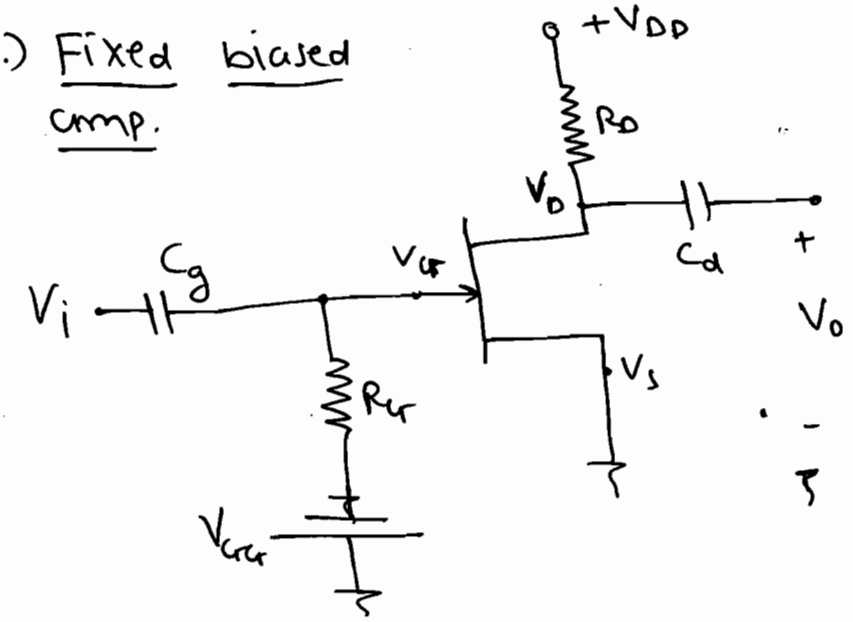
⇒ CD and CS can not be used as the current amplifier. because FET has high input impedence and o/p impedence. i.e. at input it is open ckt. Therefore no input current. As in CD and CS input is given to the gate and when i/p is given to gate it is open ckt. and they can not be used as current amplifier. In Common gate $I_D = I_S$ so, current gain is 1. i.e. no amplification.

$$A_{Ic} = \frac{I_o}{I_i} = \frac{I_o}{I_S} = 1.$$

No current amplification.

① Common Source Configuration Amplifier.

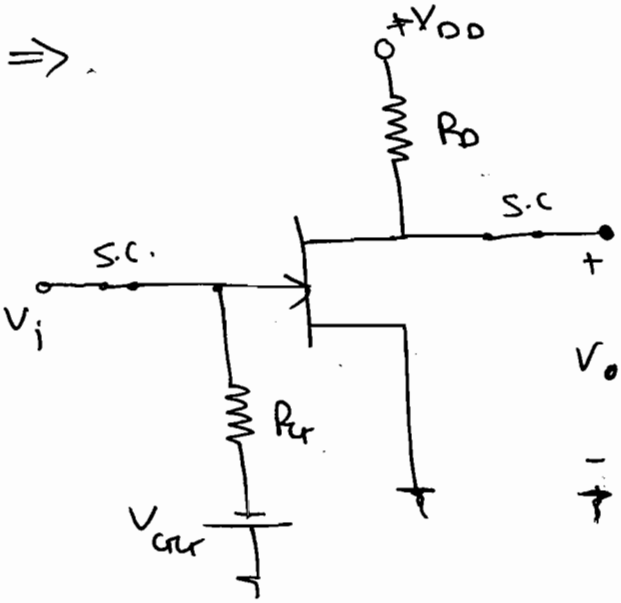
(1.) Fixed biased cmp.



Steps:

1. Short ckt the Capacitance.
2. Short ckt the d.c. power supply to Ground.
3. Identify the terminals of JFET.
4. Replace JFET with its eqn ckt.

⇒



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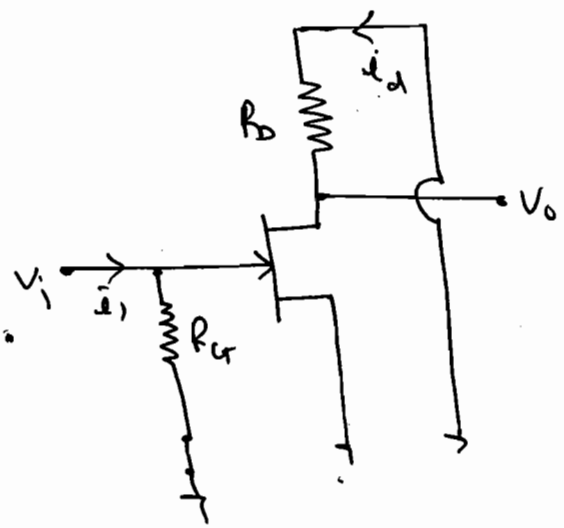
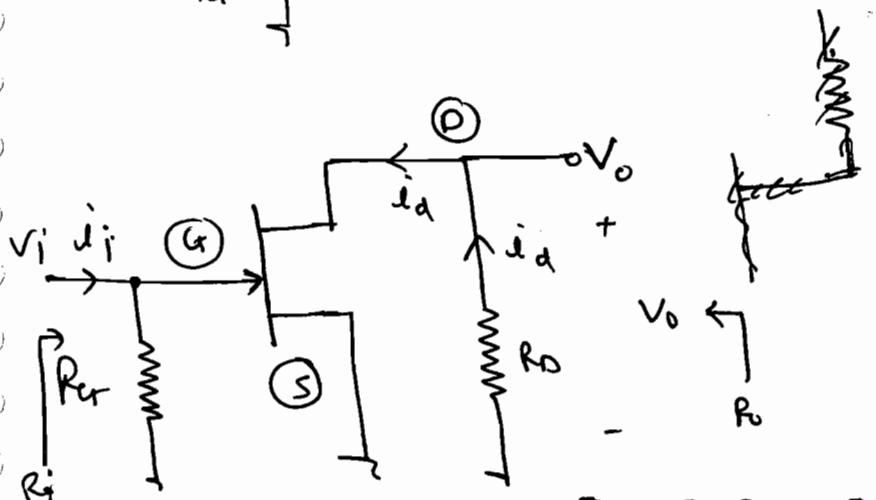
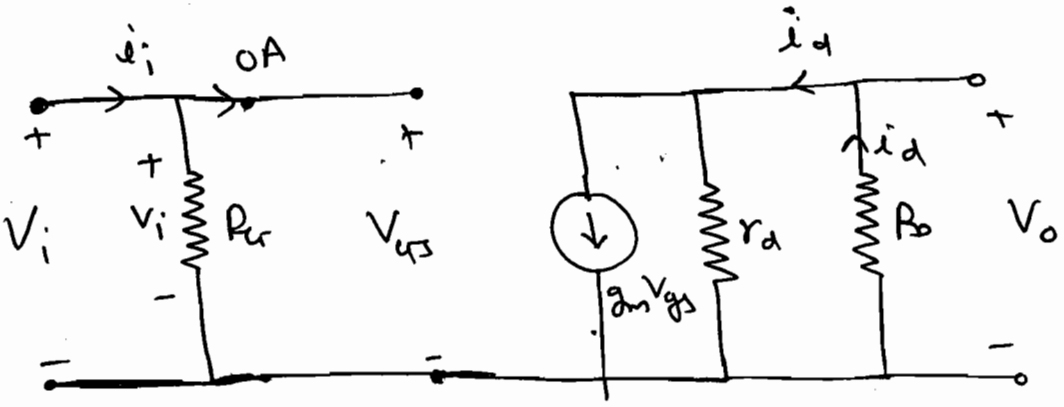




eqn ckt:



Small signal eqn ckt (or)

h-parameter eqn ckt (or)

Ac eqn ckt.

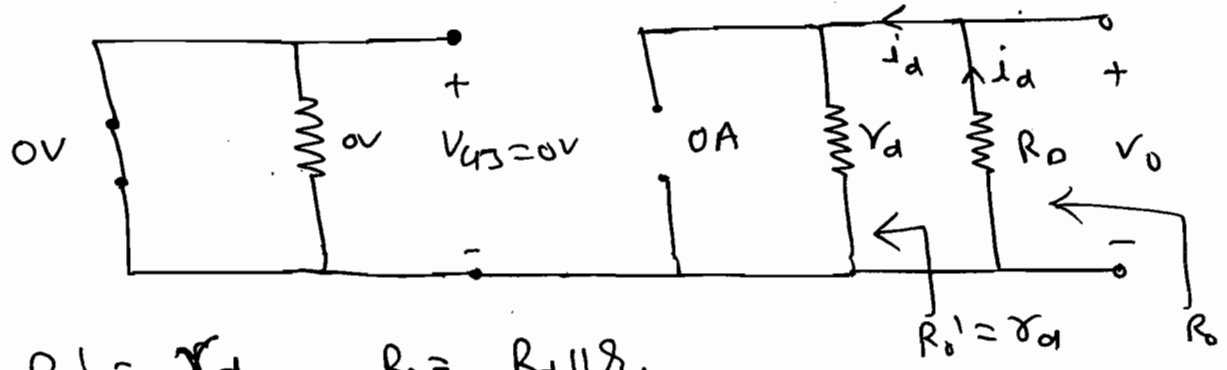
① Input Resistance (R_i):

⇒ Input resistance $R_i = \frac{v_i}{i_i} = \frac{i_i \cdot R_{cr}}{i_i} = R_{cr}$.

$\therefore \boxed{R_i = R_{cr}}$

② output Resistance (R_o):

⇒ for finding R_o make d.c. = 0.



⇒ $R_o' = r_d$, $R_o = R_d \| r_d$.

$\therefore \boxed{R_o = r_d \| R_D.}$

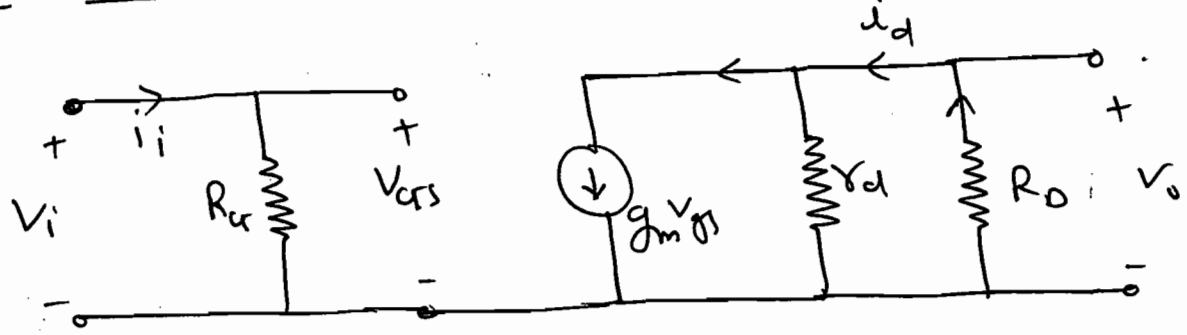
ideally $r_d = \infty$.

Practically r_d = 50k to 100k

So, for $r_d >> R_D$. (or) $r_d \geq 10 R_D$.

$\therefore$ $\boxed{R_o \approx R_D.}$

③ Voltage gain:



$\therefore$ $V_i = R_G \cdot i_i = V_{gs}$.

$\therefore$ $V_o = -g_m V_{gs} \cdot [r_d \| R_D)$.

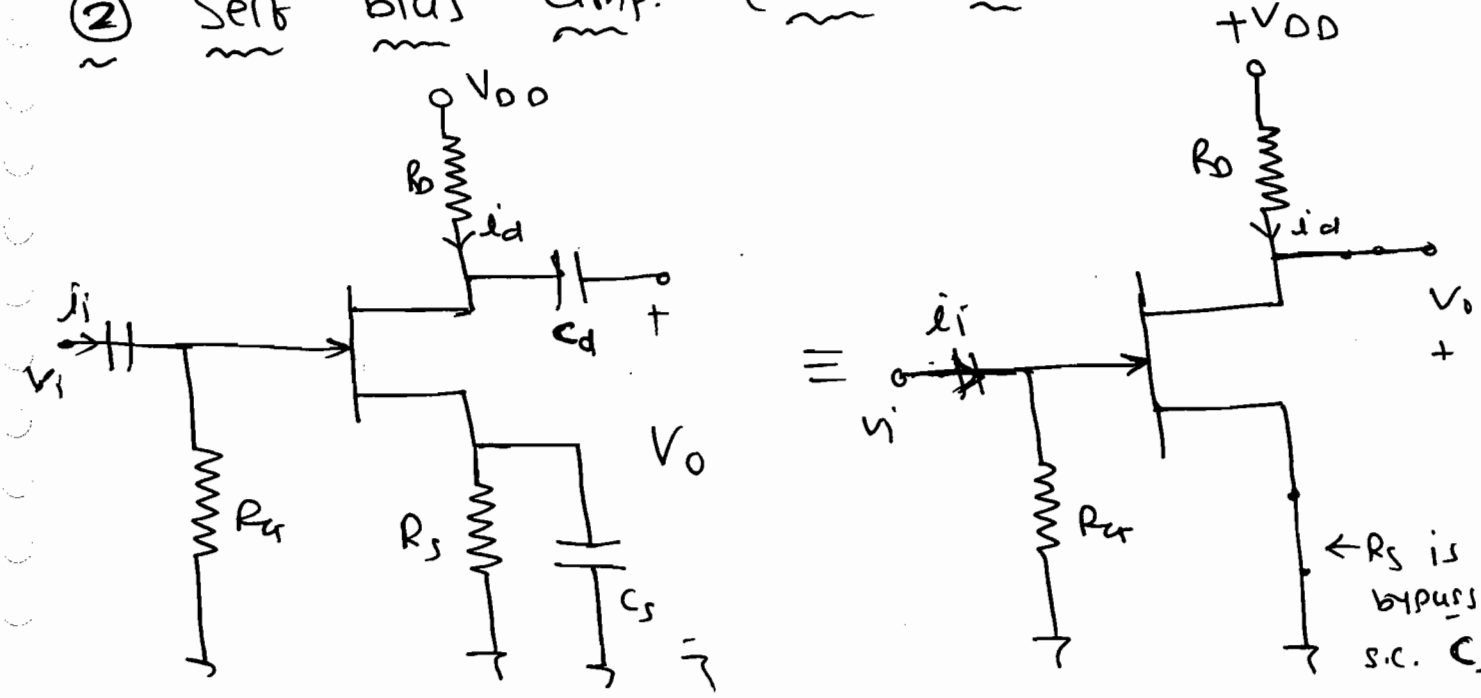
$\therefore$ $A_v = \dfrac{V_o}{V_i} = \dfrac{-g_m V_{gs} [r_d \| R_D]}{V_{gs}}$

$\therefore$ $\boxed{A_v = -g_m [r_d \| R_D].}$

But $r_d >> R_D \Rightarrow r_d \| R_D \approx R_D$.

$\therefore$ $\boxed{A_v = -g_m R_D.}$

② Self bias cmp. (with C_s):



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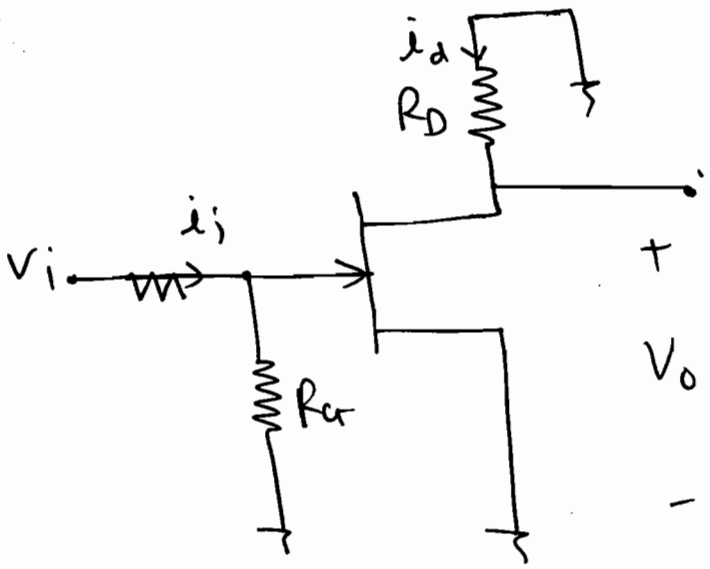

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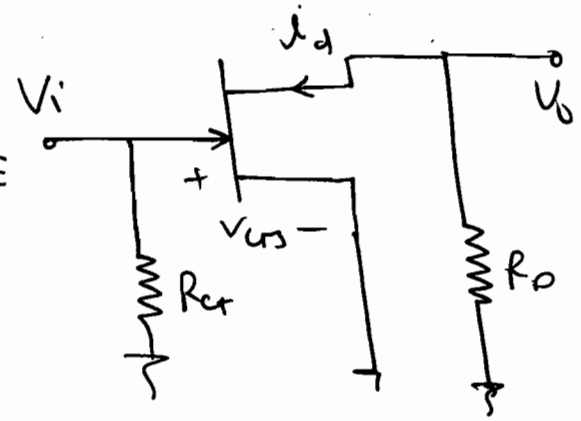
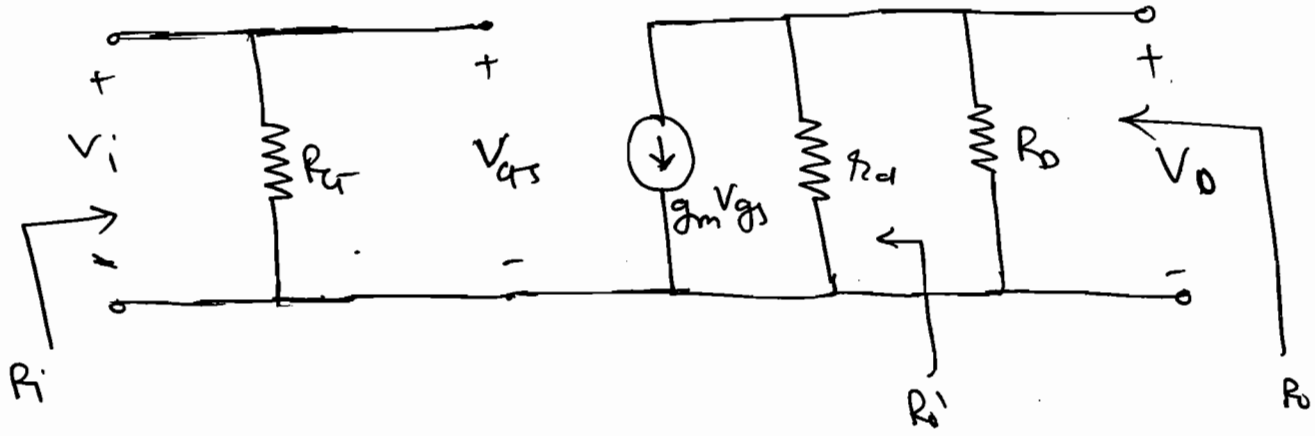




① Input Resistance:

⇒ Input Resistance $\boxed{R_i = R_G}$

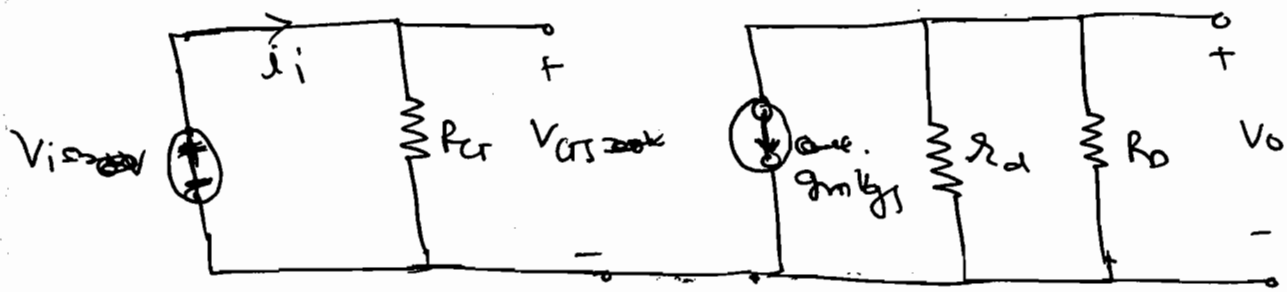
② Output Resistance:

⇒ $R_o' = R_d$, $R_o = R_d \| R_D$

$\therefore$ $\boxed{R_o = R_d \| R_D}$

$\boxed{R_o \approx R_D \quad (\because R_d >> R_D).}$

③ Voltage gain:



$$\therefore \quad V_{GS} = V_i$$

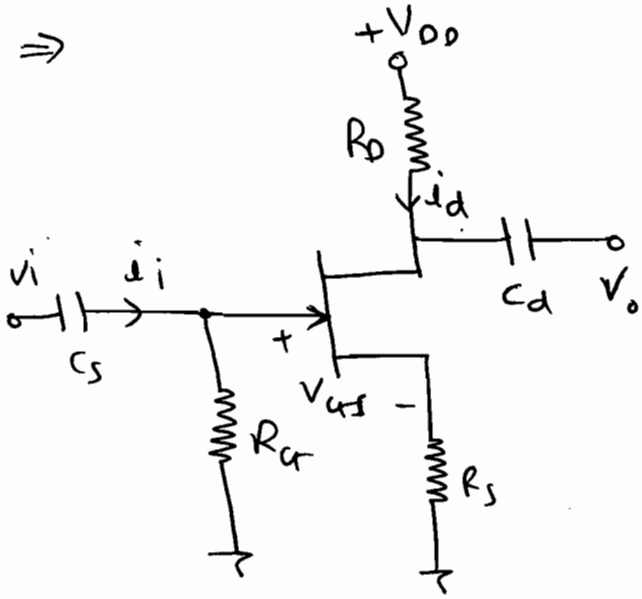
$$\therefore \quad V_o = -g_m V_{gs} [r_d \| R_D].$$

$$\therefore \quad A_V = \frac{V_o}{V_i} = \frac{-g_m V_{gs} [r_d \| R_D]}{V_{gs}}$$

$$\therefore \quad \boxed{\begin{aligned} A_v &= -g_m [r_d \| R_D] \\ A_v &\approx -g_m R_D. \quad (\because r_d >> R_D) \end{aligned}}$$

③ Self biased amp. (without C_s):

⇒



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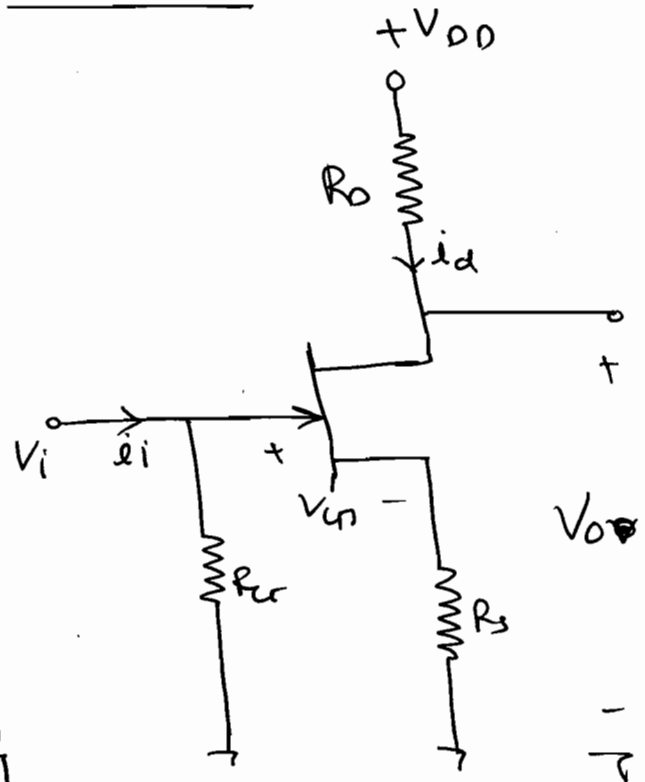

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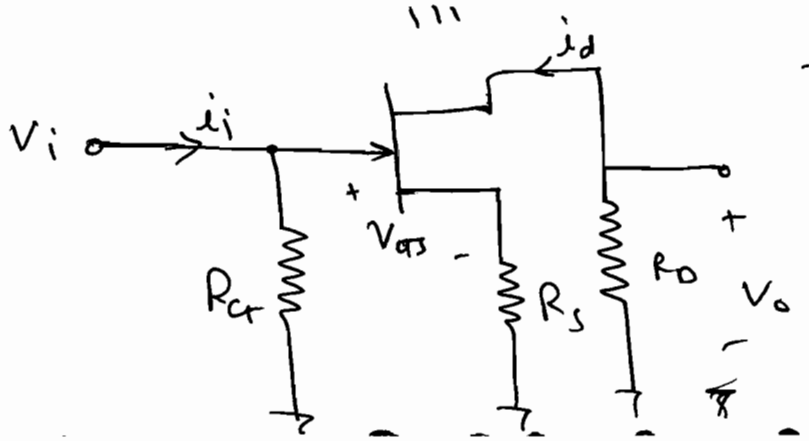

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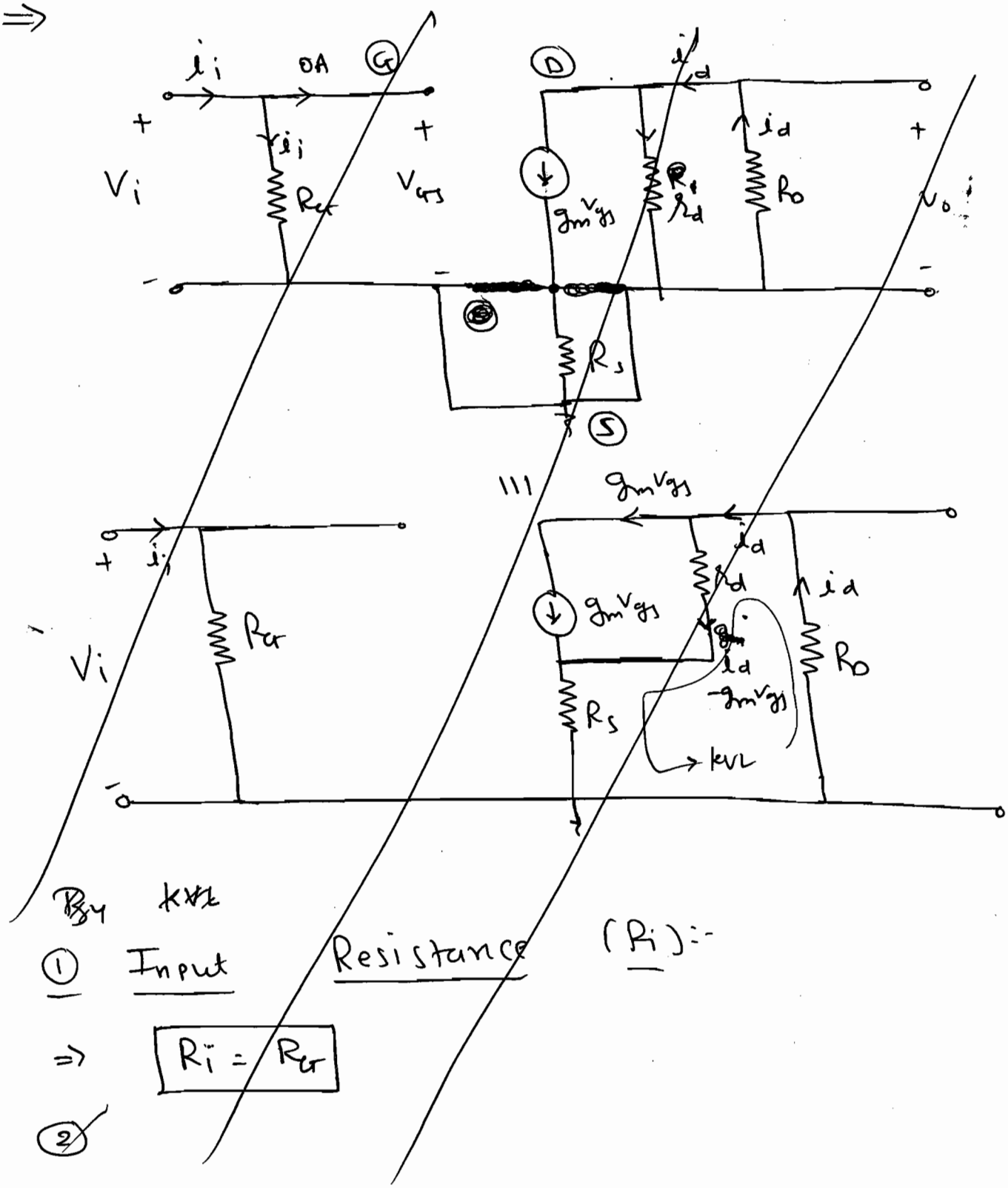


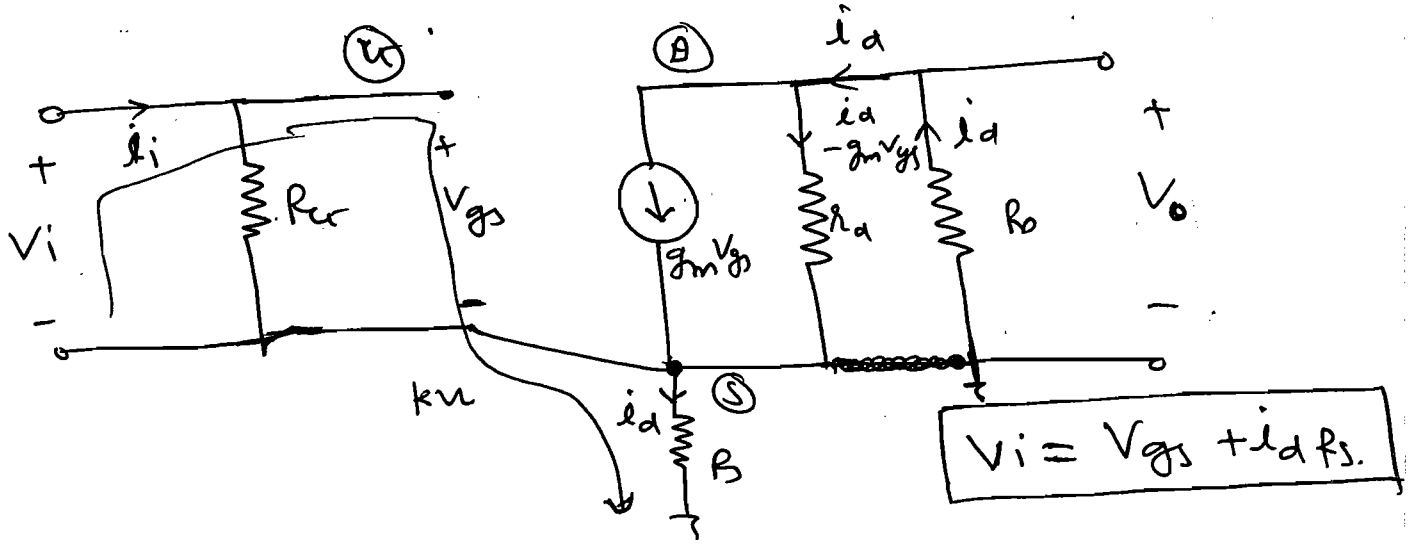
By KVL

① Input Resistance (R_i) :-

⇒ $\boxed{R_i = R_{Gr}}$

②

$\Rightarrow$

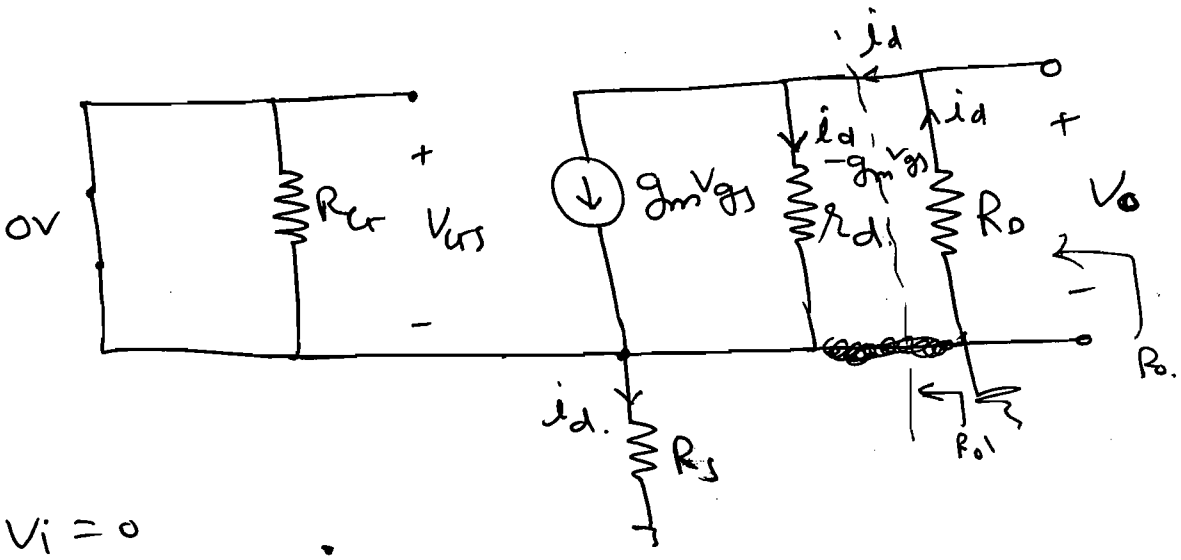


① Input Resistance (R_i):

$\Rightarrow$ Input Resistance $R_i = R_{sr}$

② Output Resistance (R_o):

$\therefore$



as $V_i = 0$

$\Rightarrow V_{GS} = -i_d R_s$.

By KVL, $V_o = r_d (i_d - g_m V_{gs}) + R_s . i_d$.

$\therefore R_o = R_D \| R_o'$

$\therefore R_o' = \frac{v_o}{i_d}$.

$\therefore \frac{V_o}{i_d} = R_o' = r_d \left(1 + g_m \frac{R_s}{}\right) + R_s$.

$R_o' = r_d + (1 + g_m r_d) R_s$.

$$\therefore \boxed{R_o = R_D \parallel \left[r_d + (1+\mu) R_s \right]}$$

$(\because \quad \mu = g_m r_d)$.

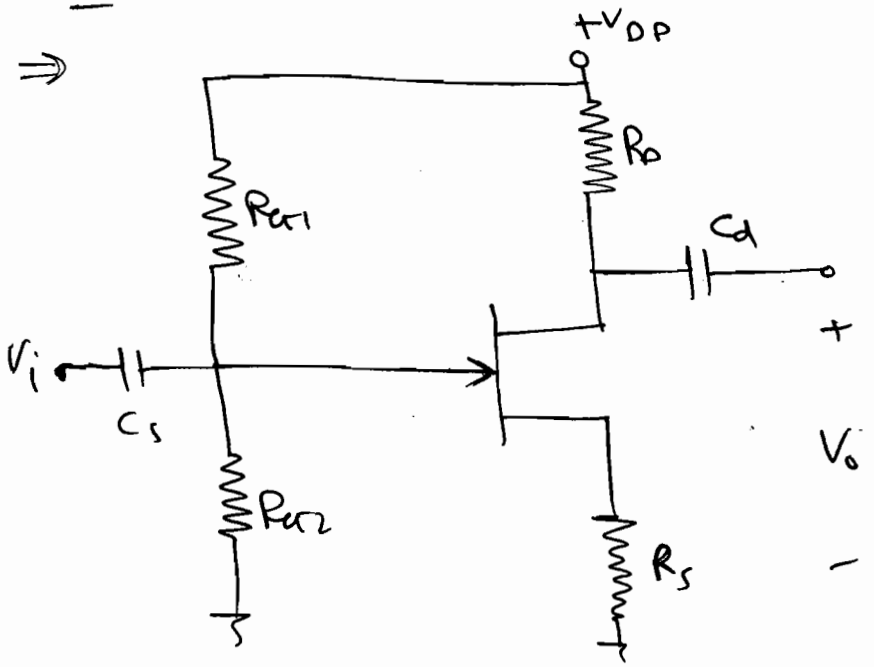
③ Voltage gain: (A_v):

$$V_i = V_{gs} + i_d R_s.$$

$$V_{gs} = V_i - i_d R_s.$$

$$\boxed{A_v = \frac{-g_m R_D}{1 + g_m R_s}}$$

④ Voltage - divider bias amp (without C_s):



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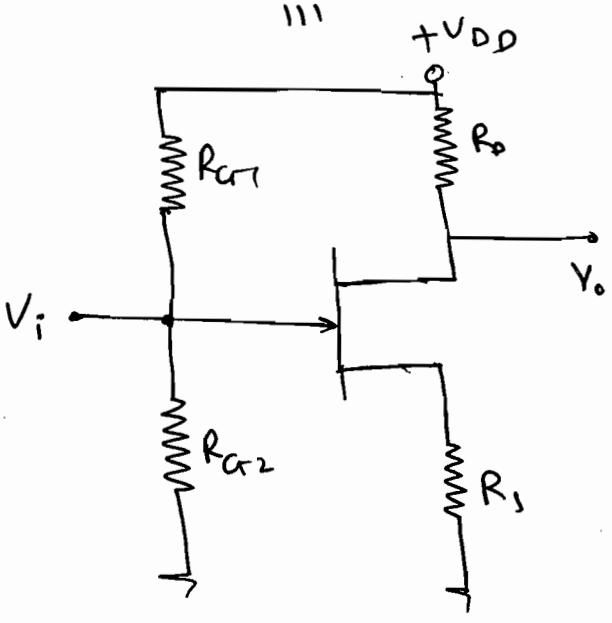

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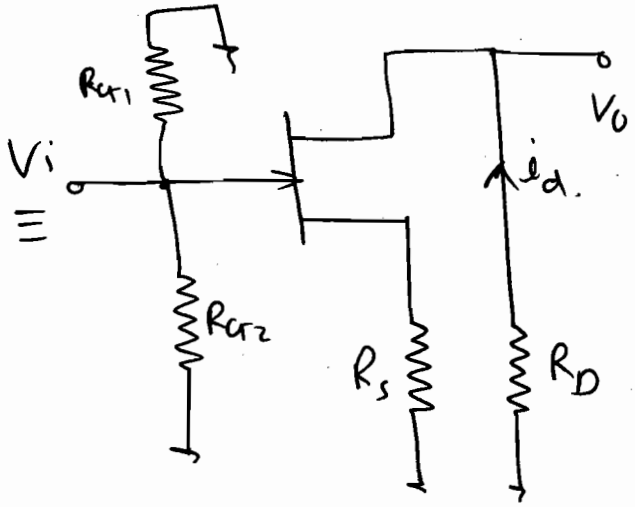
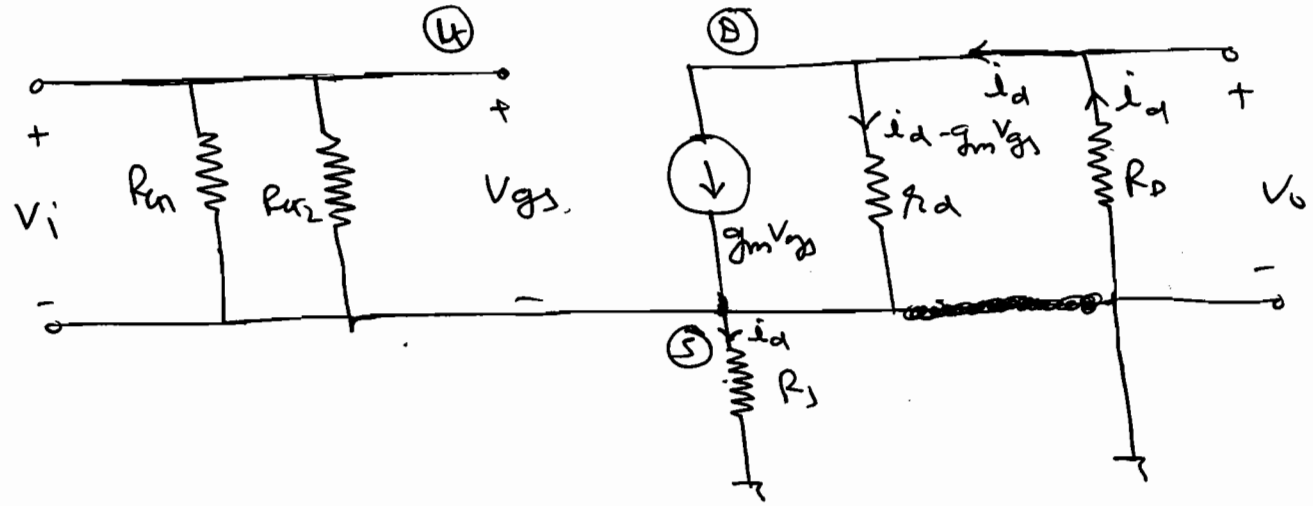




① Input Resistance (R_i):

$$\Rightarrow \boxed{R_i = R_{G1} \| R_{G2}}$$

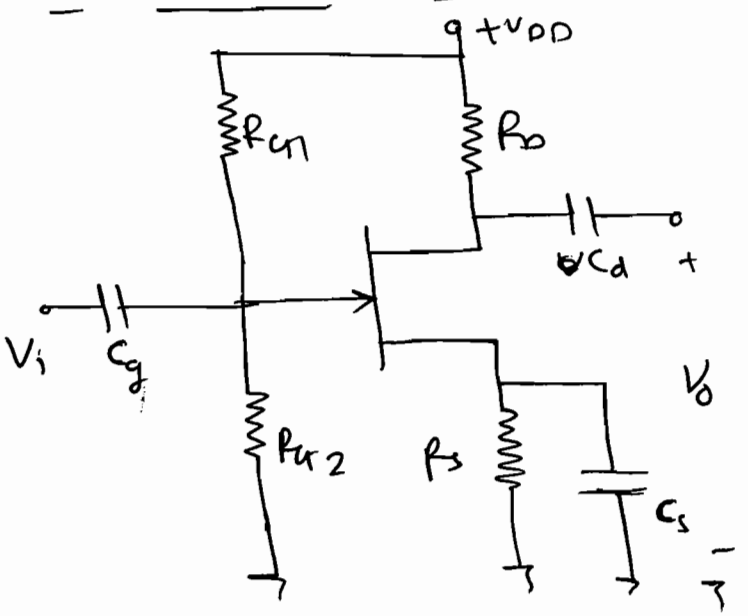
② output Resistance (R_o):

$$\Rightarrow \boxed{R_o = R_D \| [r_d + (1+\mu) R_S]. \quad (\because \mu = g_m r_d).}$$

③ Voltage gain: (A_v):

$$\Rightarrow \boxed{A_v = \frac{-g_m . R_D}{1 + g_m R_S}}$$

⑤ Voltage divider bias (with C_s):



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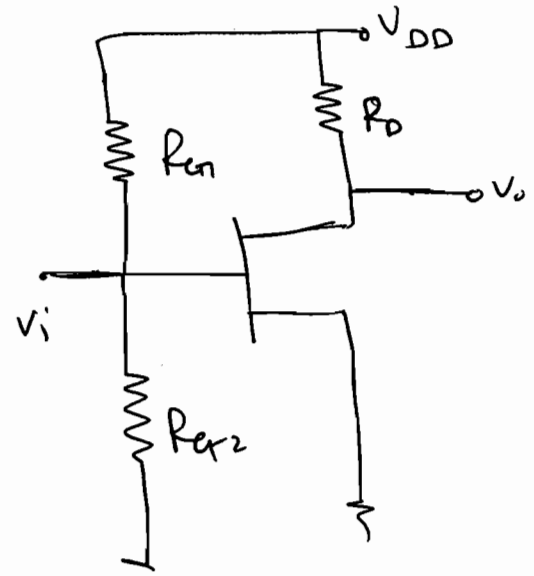

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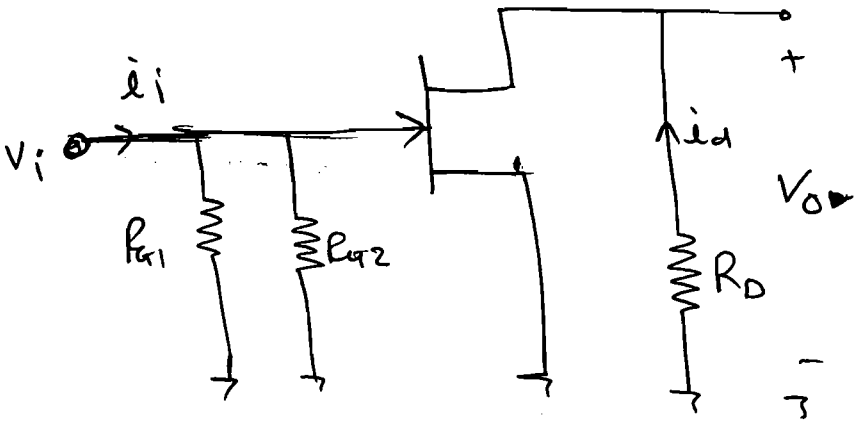

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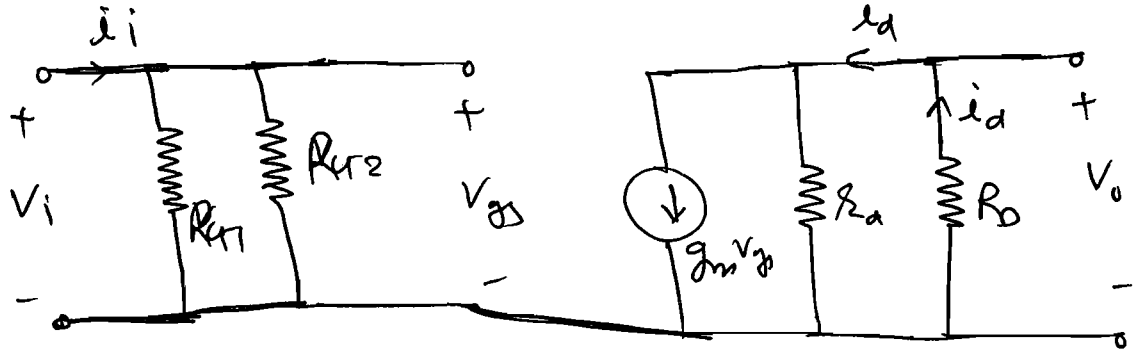


① Input Resistance:

⇒ $\boxed{R_i = R_{G1} \| R_{G2}.}$

② Output Resistance (R_o):

⇒ $R_o = R_D \| R_d$ ≈

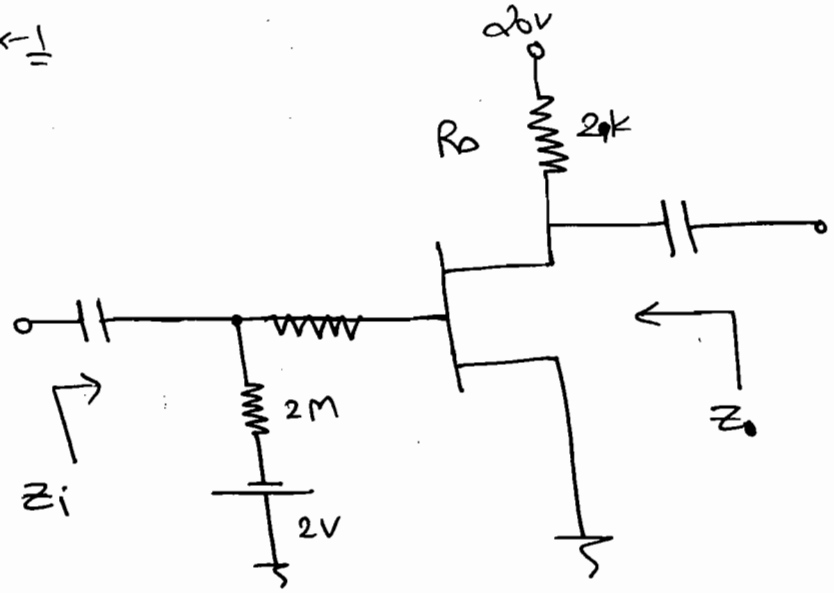
$R_o \approx R_D$ ($\because R_d >> R_D$).

③ Voltage gain (A_v):

⇒ $A_v = -g_m.(R_D \| R_d)$

$\therefore \boxed{A_v = -g_m \cdot R_D.}$

Ex-1



$R_d = 10K$

$I_{DSS} = 10mA$

$V_P = -8V$.

Q-10 $Z_i = R_i = 2M\Omega$

$Z_o = R_D \| R_d = 2K \| 10K = \frac{40}{22} = \frac{20}{11} K\Omega$.

Q-11

$$I_D = I_{DSS}\left[1 - \frac{-V_{GS}}{V_A}\right]^2$$

$$I_D = 10mA\left[1 - \frac{-2}{-8}\right]^2$$

$$\boxed{I_D = 5.625mA}$$

$V_{DS} = V_{DD} - I_D R_D$

$= 20V - 5.625mA \times 2K$

$V_{DS} = 8.75V$

Q-12

$$g_m = \left|\frac{2I_{DSS}}{-V_P}\right| \cdot \left[1 - \frac{V_{GS}}{V_P}\right].$$

$$\therefore g_m = \frac{2 \times 10m}{8} \times \left[1 - \frac{-2}{-8}\right].$$

$$\therefore \boxed{g_m = 1.875 \text{ mA/V}}$$

Q-13

$$A_V = -g_m (R_D \| R_d).$$

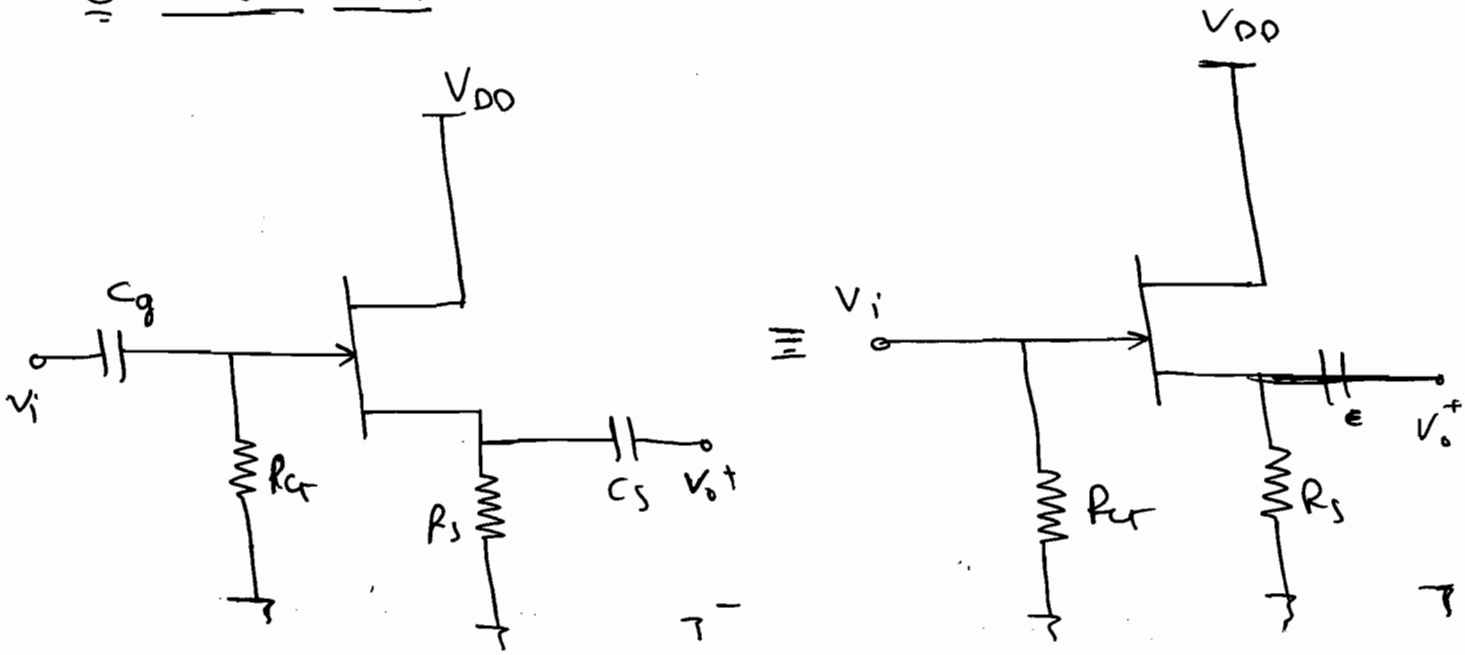
$$A_V = -1.875m\left(\frac{20K}{11}\right).$$

$$\boxed{A_V = -3.4}$$

Parameters	Fixed bias amp	Self bias amp		Voltage divider amp.	
		with C_s	without C_s	with C_s	without C_s
1. R_i	$R_i = R_G$	$R_i = R_G$	$R_i = R_G$	$R_i = R_{G1} \| R_{G2}$	$R_i = R_{G1} \| R_{G2}$
2. R_o	$R_o = R_D \| r_d$ $R_o \approx R_D$	$R_o = R_D \| r_d$ $\approx R_D$	$R_D \| [r_d + (1+\mu)R_s]$	$r_D \| R_D$ $\approx R_D$	$R_D \| [r_d + (1+\mu)R_s]$
3. A_v	$-g_m(R_D \| r_d)$ $= -g_m \cdot R_D$	$-g_m(R_D \| r_d)$ $= -g_m R_D$	$\frac{-g_m R_D}{1+g_m R_s}$	$-g_m R_D$	$-\frac{g_m R_D}{1+g_m R_s}$

② Common Drain Amplifier:

① self biased:



$$\Rightarrow R_i = R_G$$

$$R_o = r_d \,||\, R_S \,||\, \frac{1}{g_m}$$

if $r_d >> R_S$

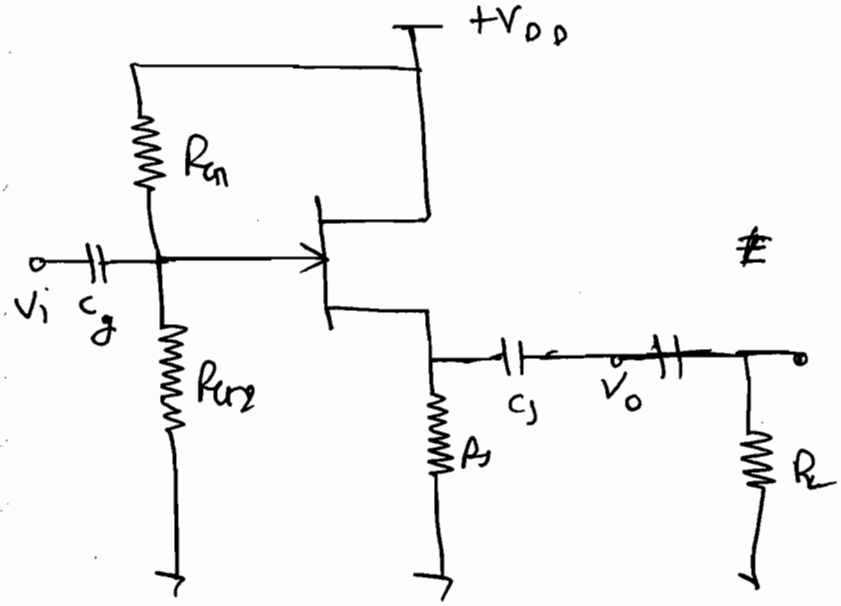
$$\therefore R_o = R_S \,||\, \frac{1}{g_m}$$

$$V_o = \frac{g_m (r_d \,||\, R_S)}{1 + g_m (r_d \,||\, R_S)}$$

if $r_d >> R_S$

$$V_o = \frac{g_m R_S}{1 + g_m R_S}$$

② Voltage divider:



→ $R_i = R_{G1} \| R_{G2}$

$R_o = R_S \| \frac{1}{g_m}$.

$A_V = \frac{g_m \cdot R_S}{1 + g_m \cdot R_S}$

if R_L is connected.

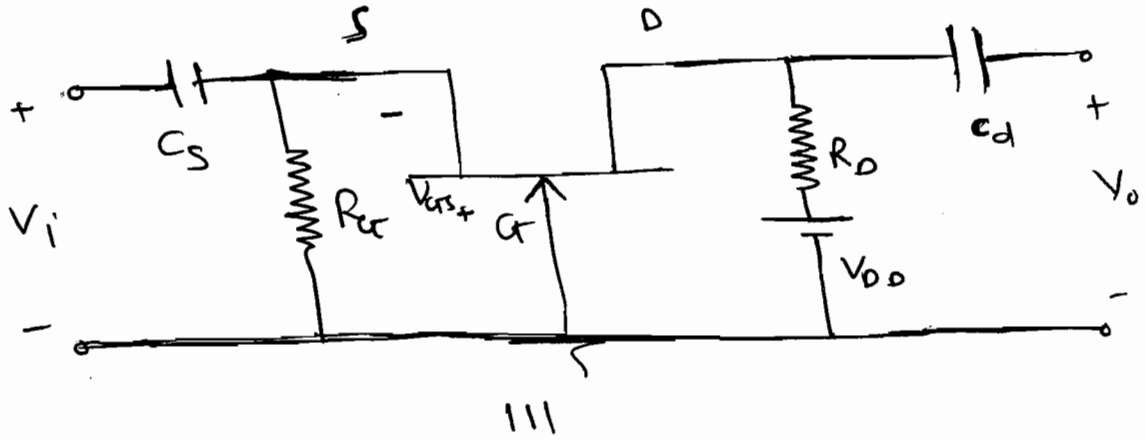
$R_i = R_{G1} \| R_{G2}$

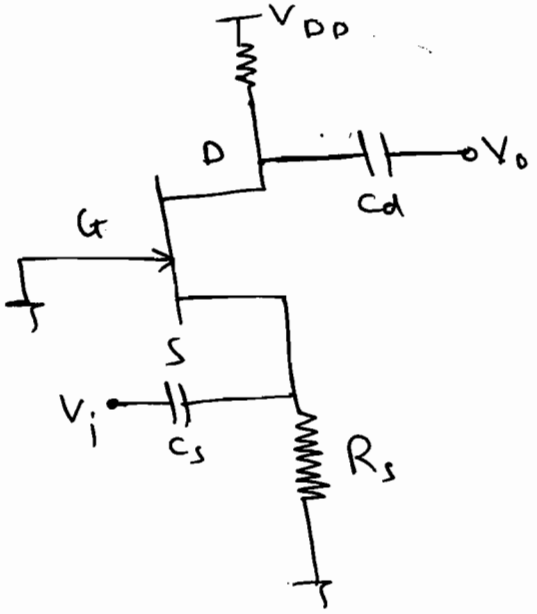
$R_o = R_S \| \frac{1}{g_m} \| R_L$

$A_V = \frac{g_m \cdot (R_S \| R_L)}{1 + g_m (R_S \| R_L)}$

③ Common gate Configuration Amp.

⇒





$R_i \cong R_S \| \frac{1}{g_m}$

$R_o = r_d \| R_D$

$A_V = g_m (r_d \| R_D)$

if $r_d >> R_D$

$R_o \approx R_D$

$A_V \approx g_m R_D$.

* BJT

CB = 0

CE = 180°

CC = 0°

FET

CG = 0°

CS = 180°

CD = 0°

① BJT:

	A_I	A_V
CB :	≈1	High
CE :	High	High
CC :	High	≈1

Voltage gain	current gain
$A_{VCC} \approx 1$	$A_{ICB} \approx 1$
$A_{VCB} > A_{VCE}$	$A_{ICC} > A_{ICE}$
$A_{CC} < A_{VCE} < A_{VCB}$	$A_{ICB} < A_{ICE} < A_{ICC}$

② FET:

Voltage gain

CD: $A_{V_D} = \frac{g_m R_s}{1 + g_m R_s} \approx 1$

Current gain

CG: $A_{ICG} = \frac{I_o}{I_s} = 1.$

CS: A_{VCS}

CG: A_{VCG}

$A_{VCG} > A_{VCS}$

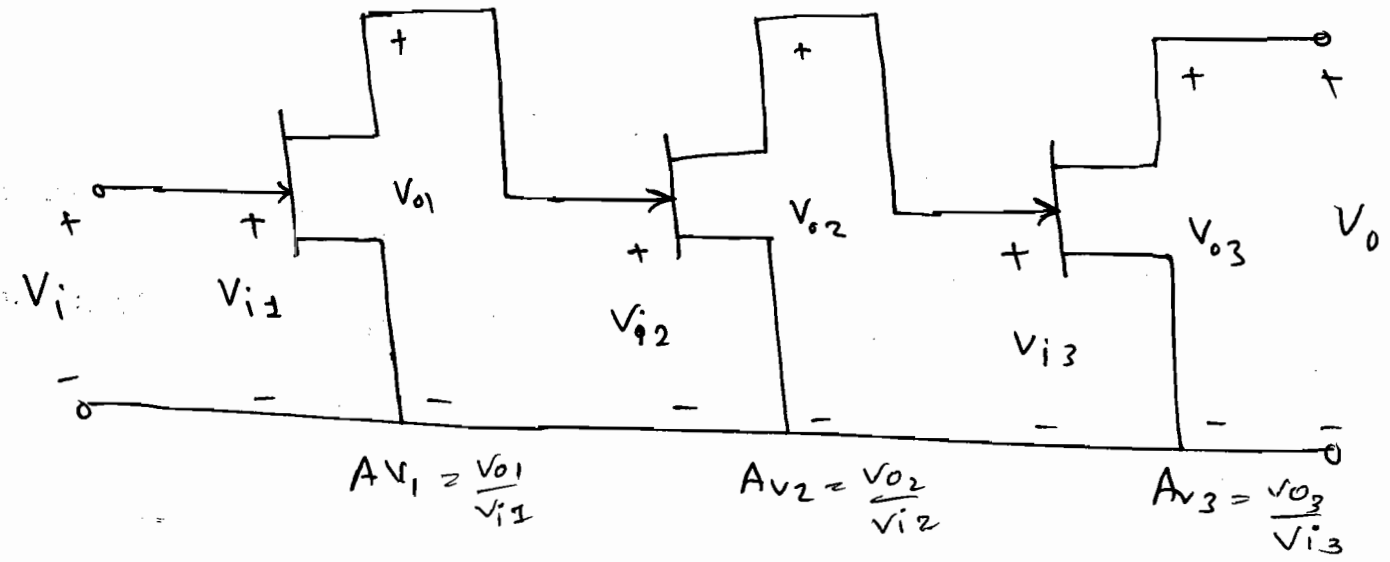
$A_{VCD} < A_{VCS} < A_{VCG}$

⇒ ☆

⇒ So, whenever we go for the multistage amplifier we should always remember it voltage gain and current. Because voltage gain ~~exact~~ ~~current~~ ~~gain~~ decide its input and output impedence. whenever we want to decide voltage amplifier max power should be transfer form one stage to another stage and for that MPTT should be apply.

☆ Multistage Amplifier:

⇒



overall gain $A_V = \frac{V_0}{V_i}$

$$A_V = \frac{V_0}{V_{03}} \times \frac{V_{03}}{V_{i3}} \times \frac{V_{i3}}{V_{02}} \times \frac{V_{02}}{V_{i2}} \times \frac{V_{i2}}{V_{01}} \times \frac{V_{01}}{V_{i1}} \times \frac{V_{i1}}{V_i}$$

$$\frac{V_0}{V_{03}} = 1, \quad \frac{V_{03}}{V_{i3}} = A_{V_3}, \quad \frac{V_{i3}}{V_{02}} = 1, \quad \frac{V_{02}}{V_{i2}} = A_{V_2}, \quad \frac{V_{i2}}{V_{01}} = 1, \quad \frac{V_{01}}{V_{i1}} = A_{V_1}, \quad \frac{V_{i1}}{V_i} = 1$$

$$\boxed{A_V = A_{V_3} \times A_{V_2} \times A_{V_1}}$$

⇒ In a multistage amplifier overall voltage gain is the product of individual stage voltage gain provided that there should not be any series resistance betⁿ two stages but shunt resistance can be allowed.

⇒ In multistage current amplifier overall current gain is the product of individual stage current gain provided that there should

not be any Shunt resistance blw two stages but series resistor can be allowed.

=> Multistage are divided into four parts:

① Cascade ② Cascode ③ Darlington ④ Parrallel.

① Cascde Connection: (for getting high voltage gain)

=> For BJT:

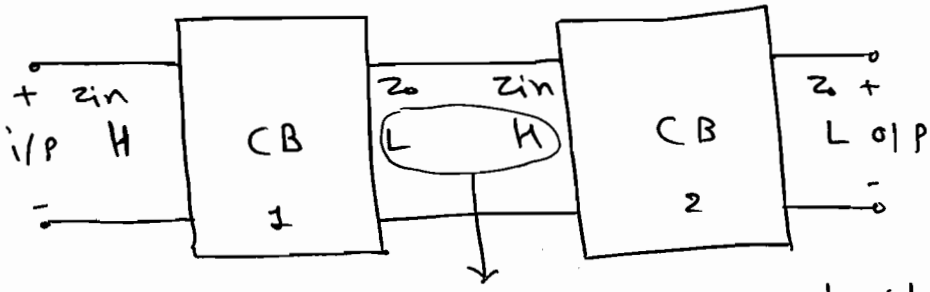
	Z_{in}	Z_o
CB:	High	Low
CE:	High	High
CC:	Low	High.

we can Connect

CB - CB
CE - CE
CC - CC.

} Possible but all are not valid.

① CB-CB:

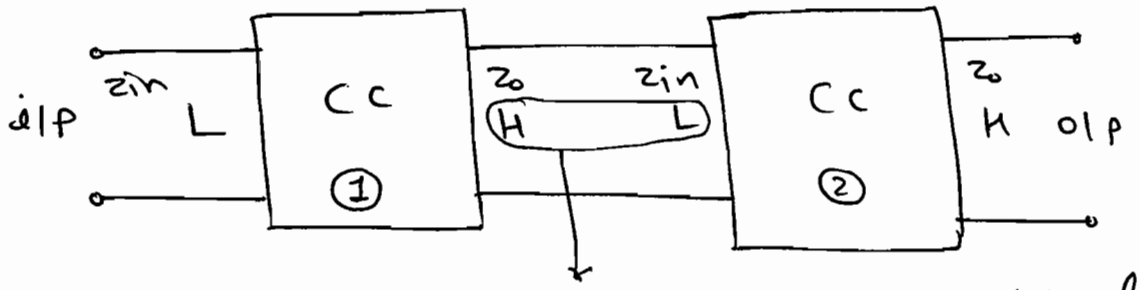


max. power not trasfer from stage 1 to 2.

So, even though CB has high voltage gain it can not be used in case-cade Connection, for overall high voltage gain.

② CC - CB:
=

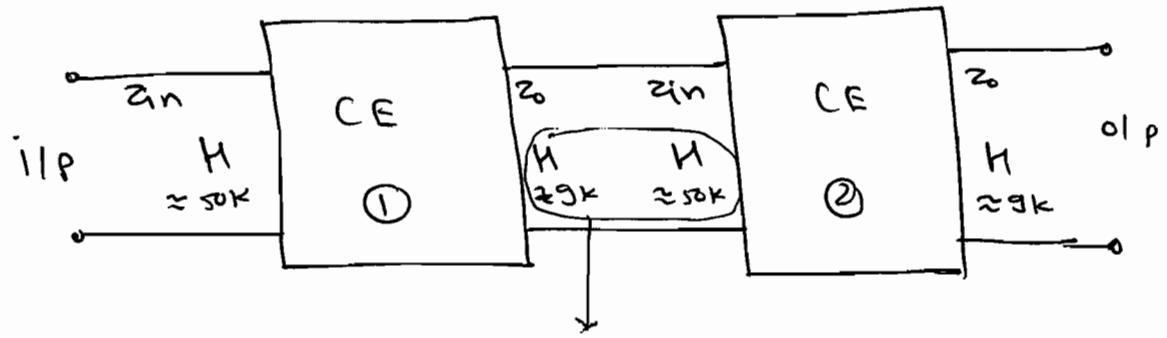
⇒



max. power will not be transfer from stage ① to ②.

So, CC has voltage gain almost 1 and it also not used in voltage amp.

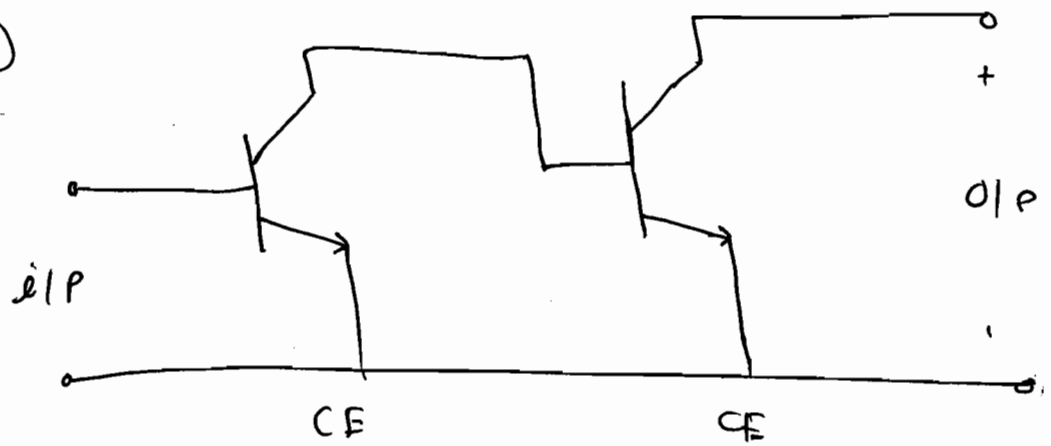
③ CE - CE:



due to this we can get max. power transfer from stage -① to ②.

⇒ Therefor, In most of the practical application we use CE - CE cascade amplifier.

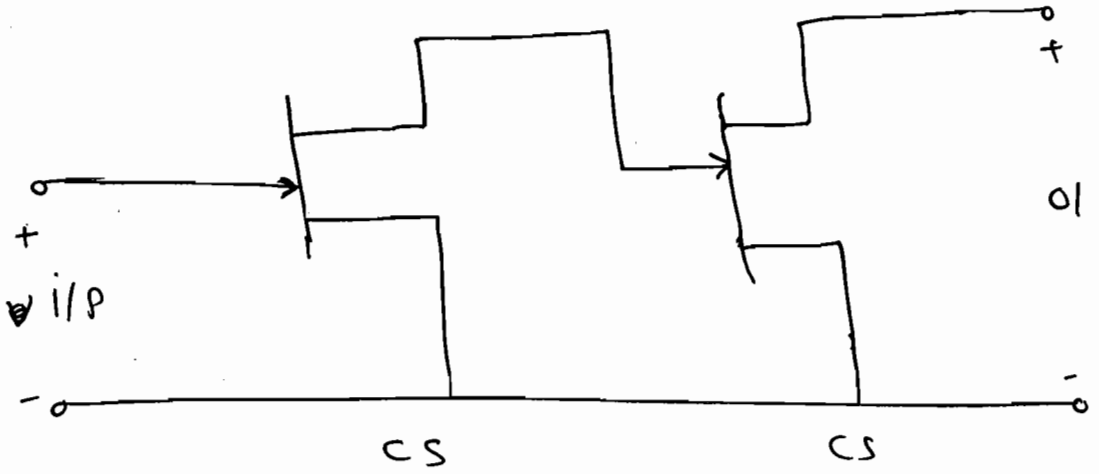
①



② For FET:

⇒ Same concept is applied into FET.

① So, only one possible way is CS-CS Casecade connection for voltage amplifier.



② Case-Cade Connection: (for ↑ getting. High Bandwidth & i/p impedence)

⇒ ① For BJT:

CE CB CC

⇒ As there are three Configuration (CE, CB, CC), there are six possible way to make Case-cade connection.

① CE - CB Vaiid
H (H) — (H) L

② CE - CC Invaiid.
H (H) × (L) H

③ CB - CC vaiid.
H (L) — (L) H

④ CB - CE
H (L) × (H) H
✗ not vaiid

⑤ CC - CE vaiid
L (H) — (H) H

⑥ CC - CB. vaiid.
L (H) — (H) H

⇒ Among six possibility, four are valid for wide band structure and Cascode Connection.

From that,

We can say that CB-CC & CC-CB are same because it is a just matter of order. i.e. first CB (or) CC no matter, it work same.

⇒ But, in CB-CC, ~~impact~~ ~~im~~

z_{in} = High, z_o = high whereas

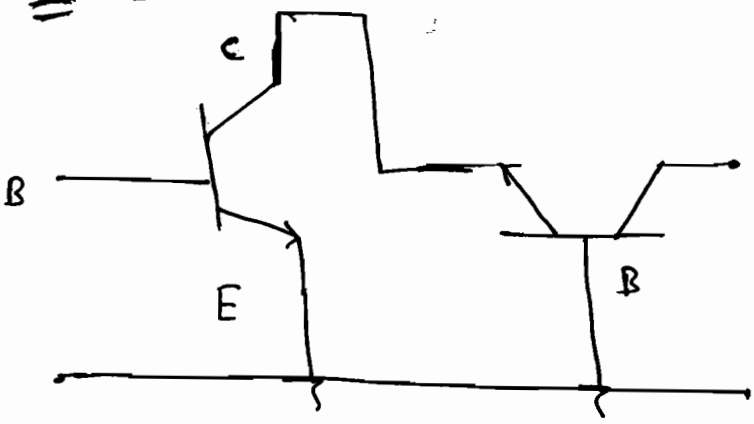
in CC-CB

z_{in} = Low, z_o = high. so it provide better gain Compare to CB-CE.

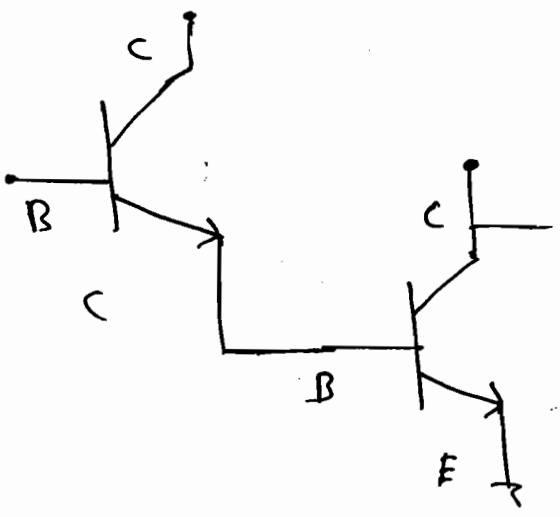
so, wide band structure, (or) Cascode Connections are.

① CE-CB ② CC-CE ③ CC-CB.

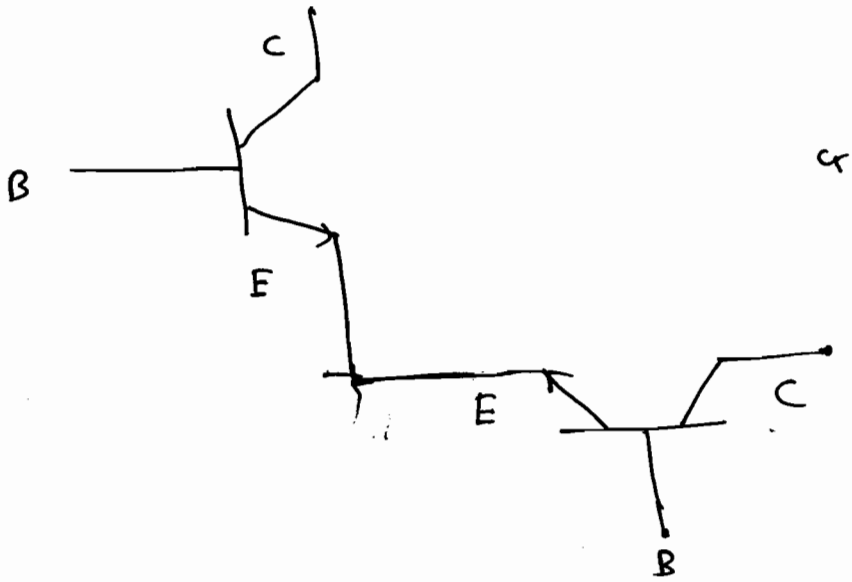
① CE-CB:



② CC-CE

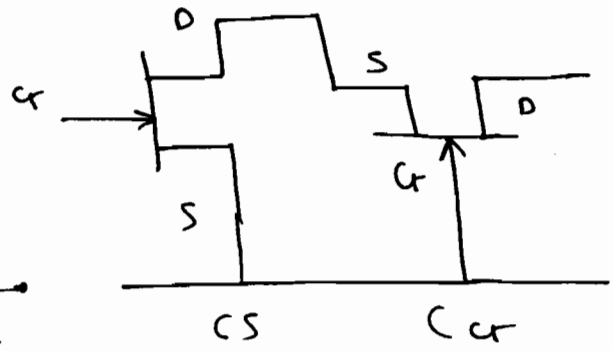


③ CC-CB:



② For JFET:

⇒ CS-CG

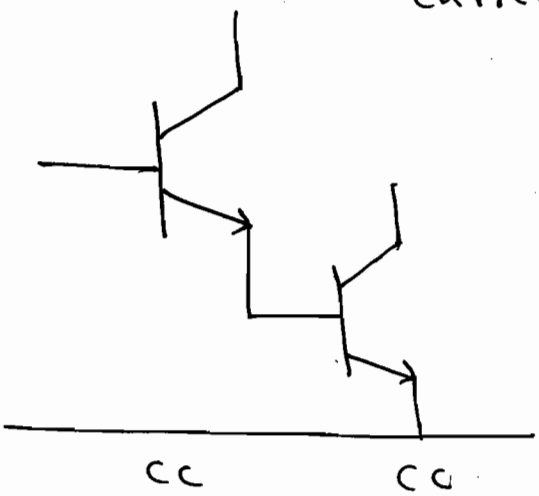


CD-CS
CD-CG

③ Darlington Connection: (for getting high current gain)

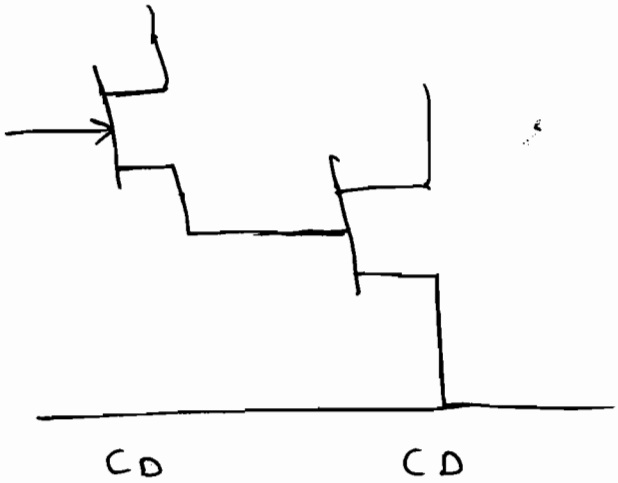
① For BJT

CC-CC For large current gain



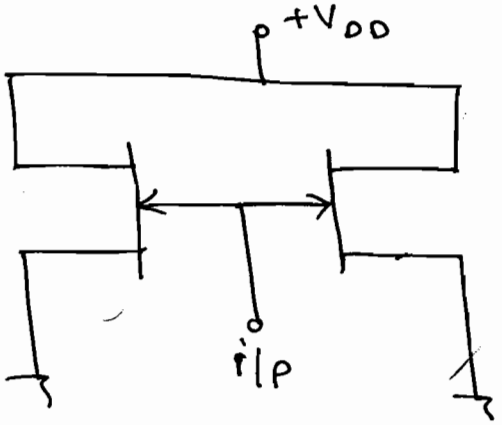
② For FET

CD - CD.

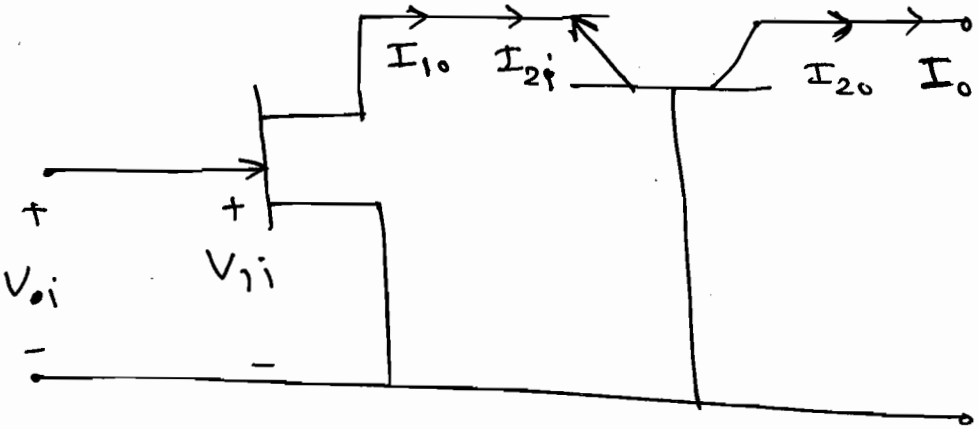


④ Parallel: (to increasing current Rating)

⇒ FET



Q-1 For the Ckt shown in the fig. FET has trans conductance of 5 mA/V and BJT has a ~~CB~~ CB current gain 0.8. Calculate overall trans conductance of the Composite amp.



Soln:

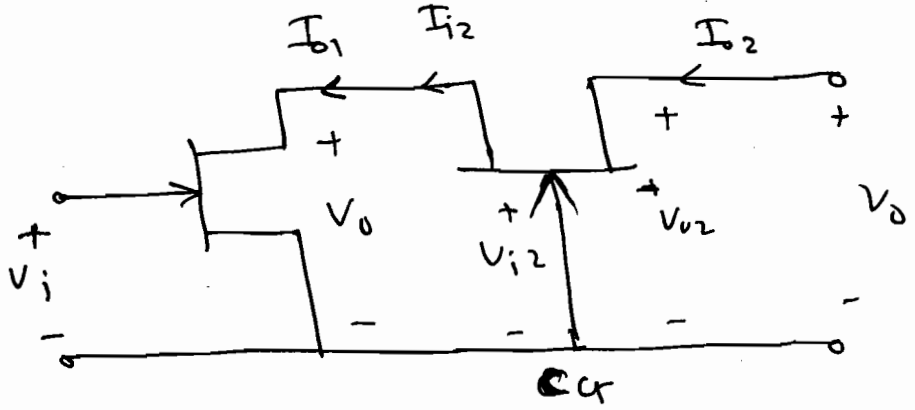
$$\therefore g_m = \frac{I_o}{V_i} = \frac{I_o}{I_{20}} \times \frac{I_{20}}{I_{2i}} \times \frac{I_{2i}}{I_{1o}} \times \frac{I_{1o}}{V_{1i}} \times \frac{V_{1i}}{V_{oi}}$$

$\frac{I_o}{I_{20}} = 1$, $\frac{I_{20}}{I_{2i}} = 0.8$, $\frac{I_{2i}}{I_{1o}} = 1$, $\frac{I_{1o}}{V_{1i}} = 5\,mA/V$, $\frac{V_{1i}}{V_{oi}} = 1$

$$\therefore g_m = 0.8 \times 5$$

$$\boxed{g_m = 4\ mA/V.}$$

Q-2



CC

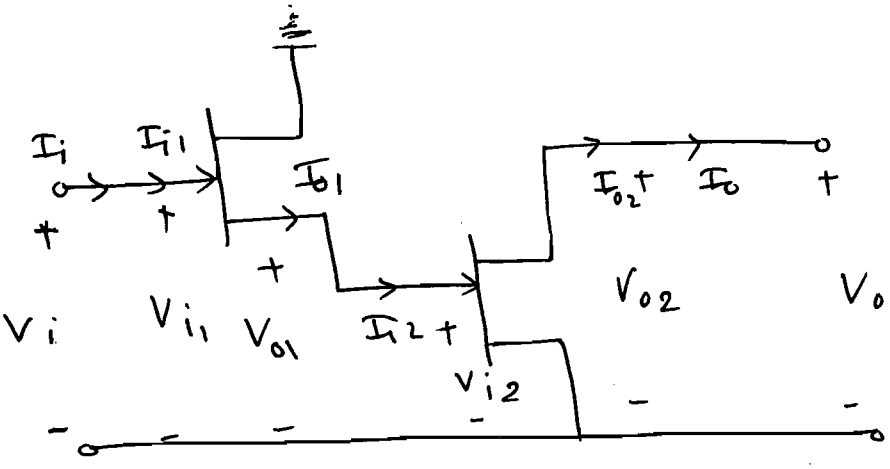
⇒ For the Ckt shown in the fig. transistor M_1 & M_2 has trans conductances of g_{m1} & g_{m2} Calculate the overall trans conductances of the Composite amplifier.

$\Rightarrow$ overall $g_m = \frac{I_o}{I_{o2}} \times \frac{I_{o2}}{I_{i2}} \times \frac{I_{i2}}{I_{o1}} \times \frac{I_{o1}}{V_{i1}} \times \frac{V_{i1}}{V_i}$

$\frac{I_o}{I_{o2}} = 1$, $\frac{I_{o2}}{I_{i2}} = 1$ (current mirror), $\frac{I_{i2}}{I_{o1}} = 1$, $\frac{I_{o1}}{V_{i1}} = g_{m1}$, $\frac{V_{i1}}{V_i} = 1$

$$\boxed{g_m = g_{m1}}$$

Q-3 For the ckt shown in the figure transistor M_1 & M_2 has transconductance of g_{m1} & g_{m2}. Calculate overall trans conductance.



Soln:

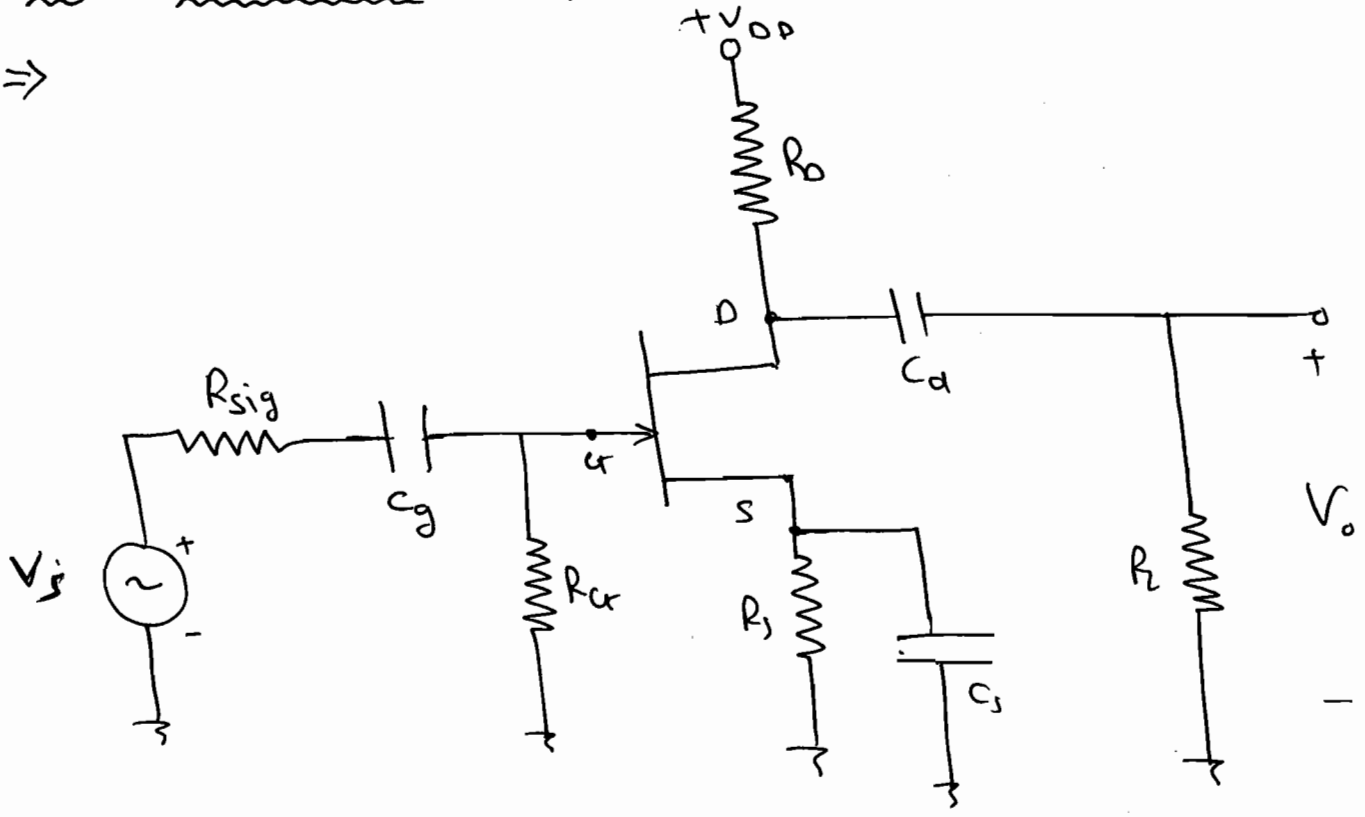
$$g_m = \frac{I_o}{V_i} = \frac{I_o}{I_{o2}} \times \frac{I_{o2}}{V_{i2}} \times \frac{V_{i2}}{V_{o1}} \times \frac{V_{o1}}{V_{i1}} \times \frac{V_{i1}}{V_i}$$

$\frac{I_o}{I_{o2}} = 1$, $\frac{I_{o2}}{V_{i2}} = g_{m2}$, $\frac{V_{i2}}{V_{o1}} = 1$, $\frac{V_{o1}}{V_{i1}} = 1$, $\frac{V_{i1}}{V_i} = 1$

$\therefore$ $$\boxed{g_m = g_{m2}}$$

✡ Frequency Response Analysis:

⇒



⇒ C_g, C_d & C_s: Coupling and bicpass cap.

$$X_c = \frac{1}{\omega C} = \frac{1}{2\pi f C}$$

DC: $f = 0 \Rightarrow X_c = \infty$ So, O.C for D.C.

* C_g:

⇒ It blocks the d.c. signals enters from source to input stage of the ampiifier.

⇒ It blocks the d.c. signals entors from the i/p stage of the ampiifier to the source.

⇒ It isolates the input stage of the amp from the source d.c. point of view i.e. act iike a open ckt for d.c. signals.

⇒ It couples the signals from source to

input of the amplifiers. i.e. it acts like a short circuit for a.c. signals.

⇒ It avoids the loading effect due to signal resistor

* C_d: (μF)

⇒ It blocks the d.c. signals from the o/p stage of amplifier to the Load.

⇒ It isolates the o/p stage of amp. from the Load d.c. point of view. i.e. it act like a open circuit for the d.c.

⇒ It Couples the a.c. signals from the o/p stage of amplifier to the Load for a.c. signals.

* C_s:

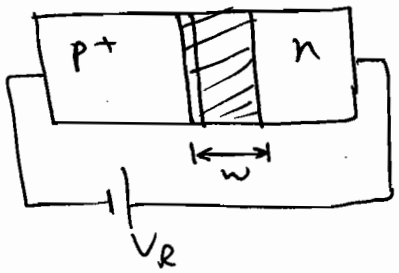
⇒ It avoids the -ve feedback due to Source resistor R_s.

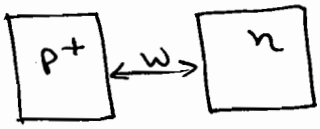
⇒ It bipasses Ac signals through it.

C_g, C_d, C_s : (μF) (4.7 μF, 10μF)

→ Always prefere short circuit for A.C. signals.

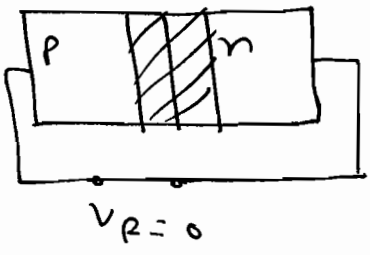
① R.B.





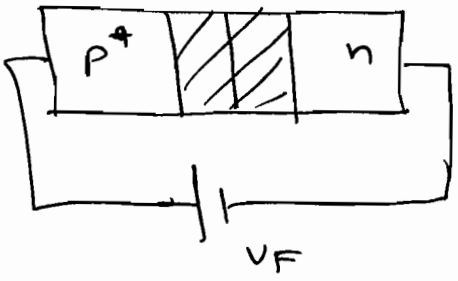
$$C = \frac{\epsilon A}{W}.$$

② O.C.



$$\epsilon_0 = \epsilon A / W.$$

③ F.B. (Diffusion Cap.).



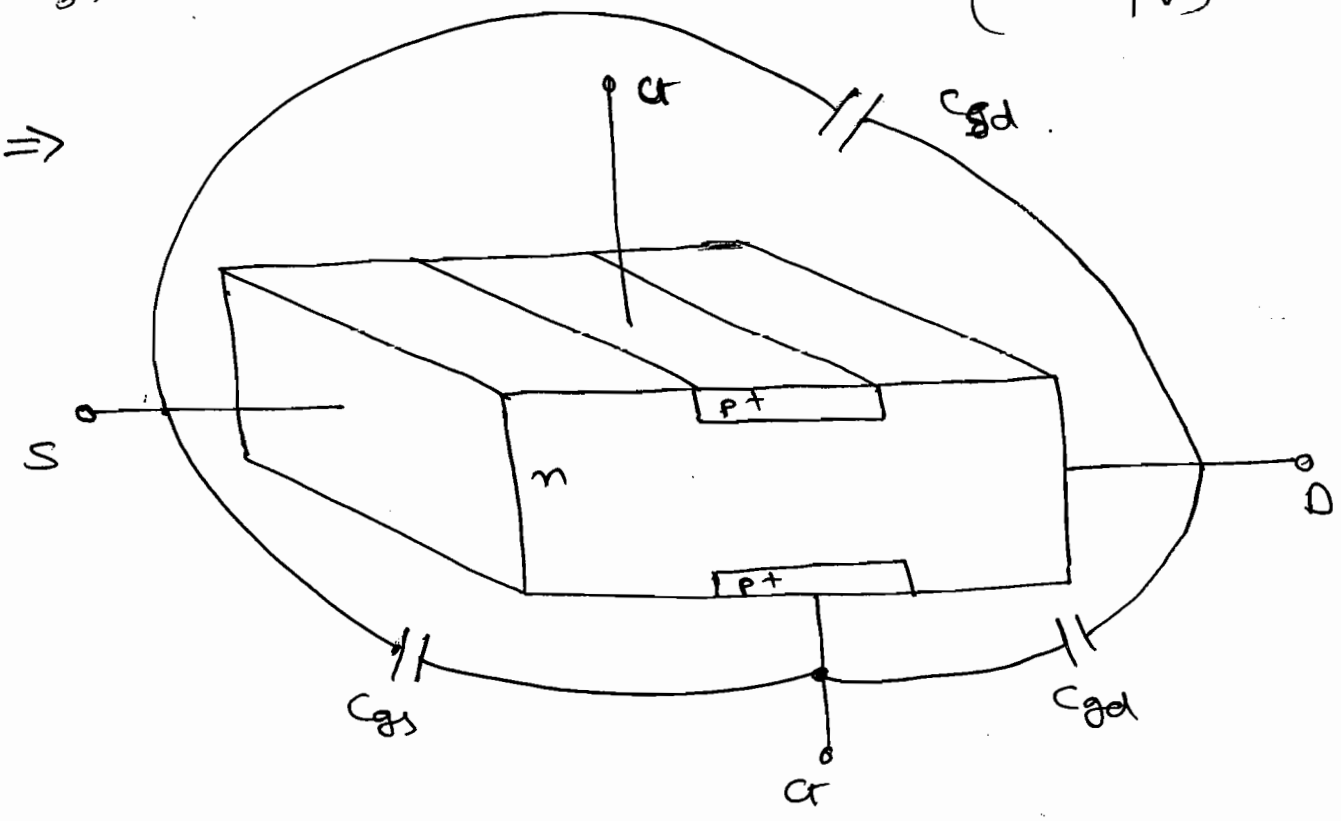
Transition Capacitance

$$C_T = \frac{C_{T0}}{\left(1 + \frac{V_R}{V_0}\right)^{1/2}}$$

$$C_j = \frac{C_{j0}}{(1 + V_R/V)^{1/2}}.$$

1/3 for linear

⇒



∴ C_{gs}, C_{gd} & C_{ds}: Junction Capacitors

⇒ Always prefere open circuit for A.C. signals.

$X_C = \frac{1}{\omega c} = \frac{1}{2\pi f c}$ and

C_{gs} C_{gd} (1 to 10 pF)

C_{sd} (0.1 to 1 pF)

* Low Freq.

⇒ Coupling Capacitor & Bypass Capacitor : O.C.

⇒ Junction Capacitors : O.C.

* Medium Freq.

⇒ Coupling Capacitor & Bypass Capacitor : S.C.

⇒ Junction Capacitors : O.C.

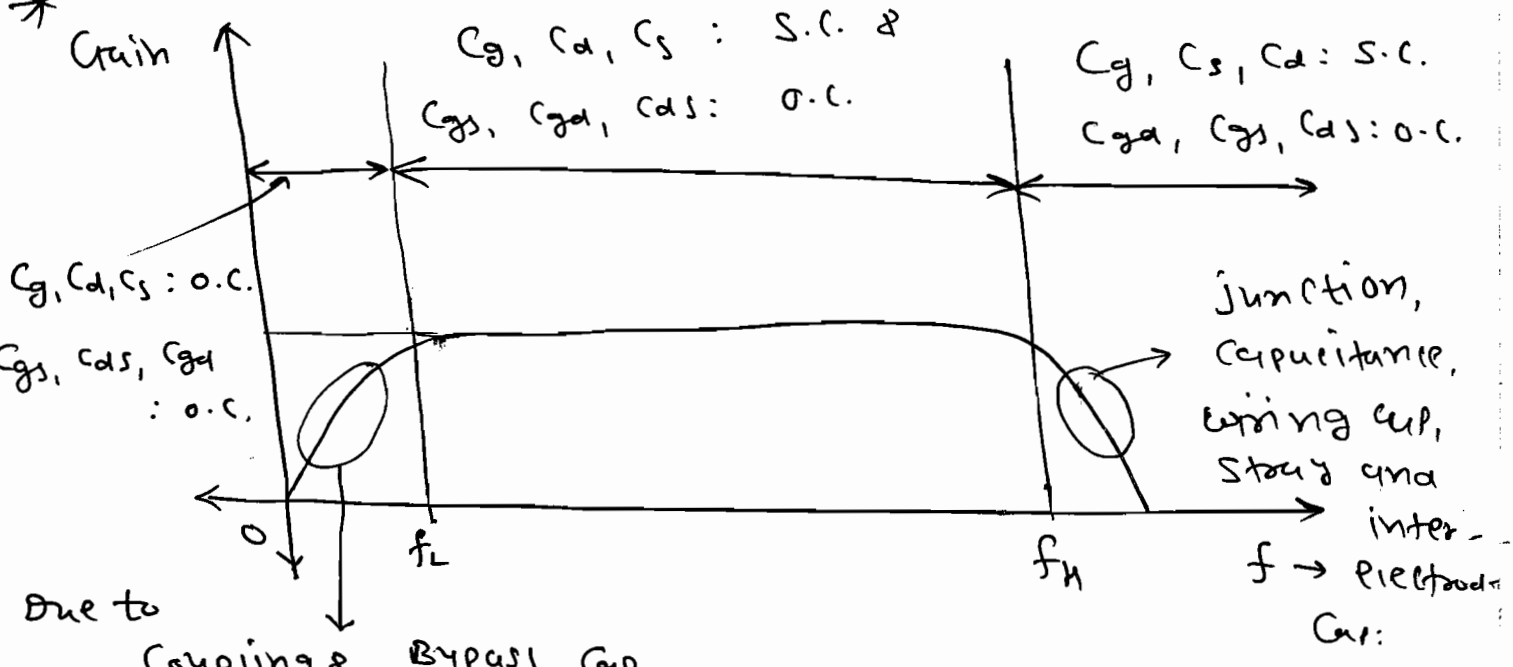
* High Freq.

⇒ Coupling & Bypass Capacitors : S.C.

⇒ ~~Coupling~~ & Junction Capacitors : S.C.

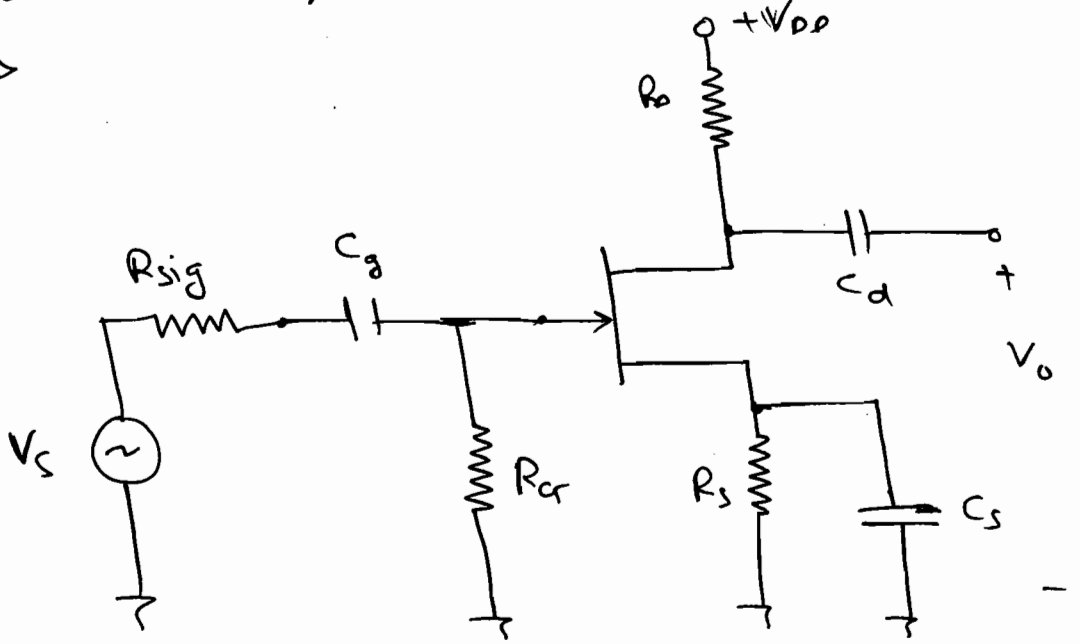
	Coupling & Bypass Capacitor	Junction Capacitors.
LF	O.C.	O.C
MF	S.C.	O.C.
HF	S.C.	S.C

*

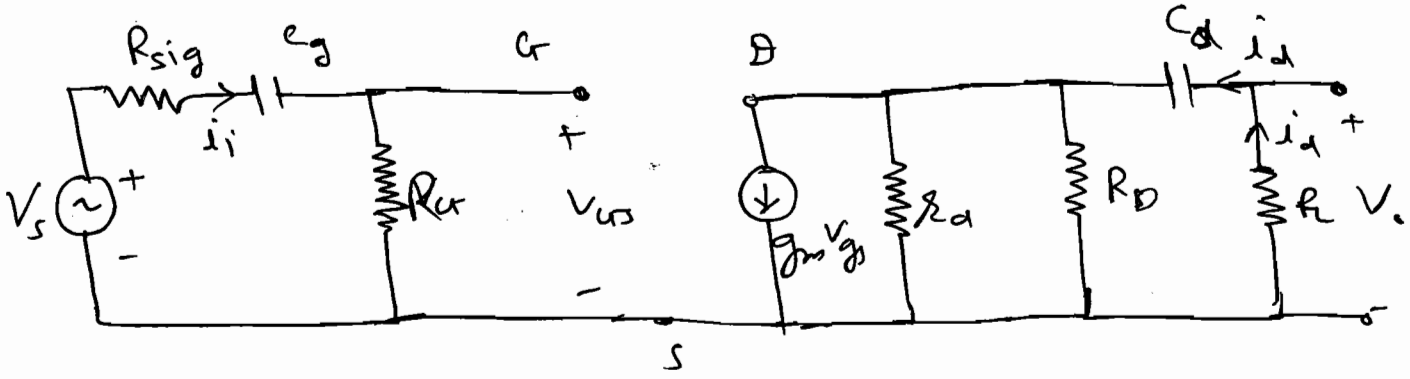


✡ Low Frequency Analysis:

⇒



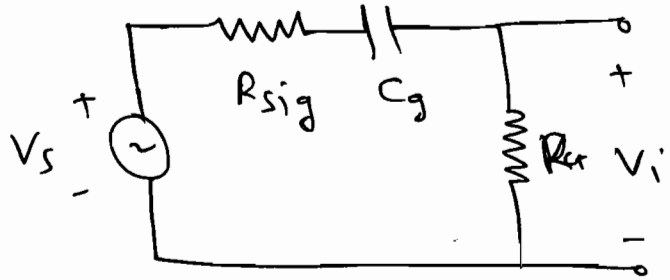
⇒ Small signal eqn (kt.



① Input side,

$V_s = V_{sig} + V_{cg} + V_i$

$\Rightarrow V_i = V_s - V_{sg} - V_{cg}$



$$H_C(j\omega) = \frac{V_i}{V_s} = \frac{R_G}{R_G + R_{sig} + \frac{1}{j\omega C_g}}$$

$$\therefore H_C(j\omega) = \frac{\frac{R_G}{R_G + R_{sig}}}{1 + \frac{1}{j\omega C_g (R_G + R_{sig})}}$$

$$\Rightarrow \quad H(j\omega) = \frac{A_0}{1 + j\,\dfrac{1}{j2\pi f C_g (R_t + R_{sig})}}$$

$$\therefore \quad \boxed{H(j\omega) = \frac{A_0}{1 + j\frac{f_L}{f}}}$$

where, $\boxed{f_L = \dfrac{1}{2\pi C_g (R_t + R_{sig})}}$

$$|H(j\omega)| = \frac{1}{\sqrt{1 + \left(\frac{f_L}{f}\right)^2}}$$

as $C_d < C_g < C_s$.

$\Rightarrow f_d > f_g > f_s$.

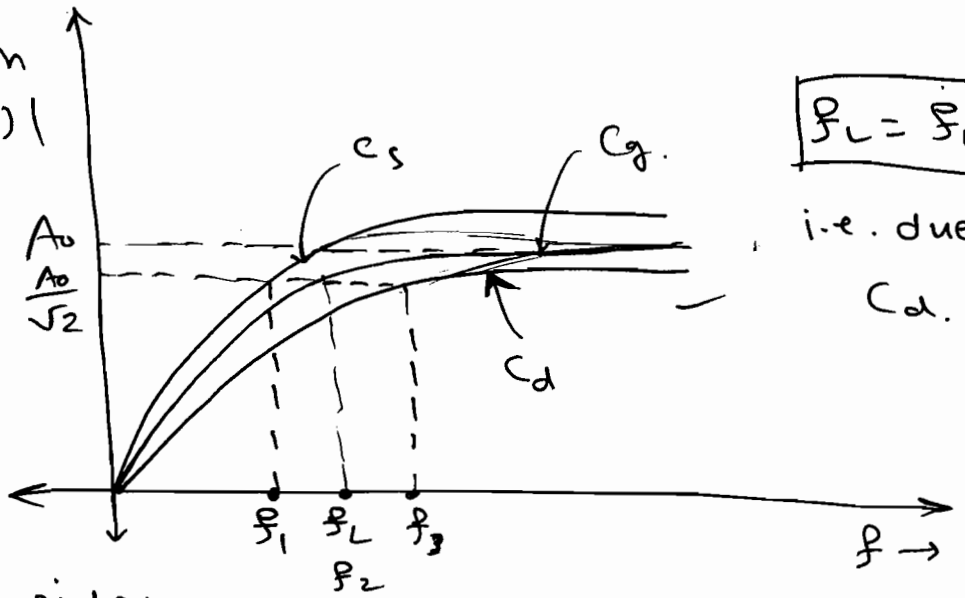
$\Rightarrow \quad f = 0 \Rightarrow H(j\omega) = 0.$

$f = f_L \Rightarrow H(j\omega) = A_0/\sqrt{2}.$

$f = f_H = \infty \Rightarrow |H(j\omega)| = A_0.$

So $\boxed{f_L = f_d = f_{L3}}$

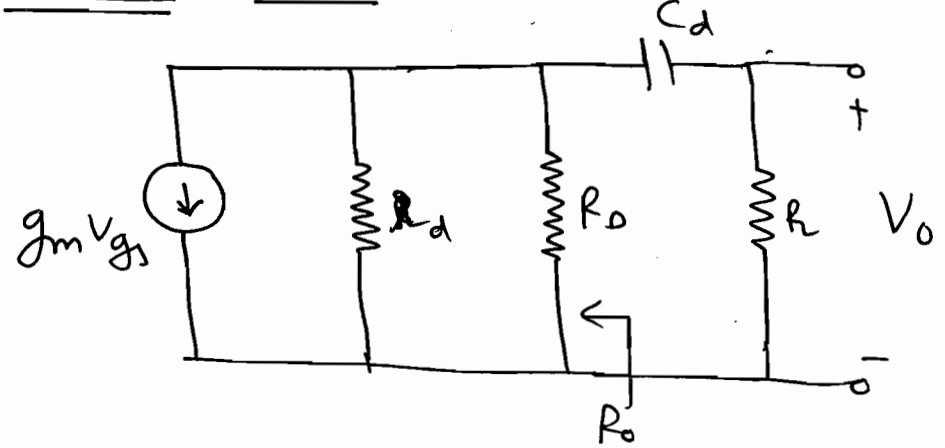
$\Rightarrow$



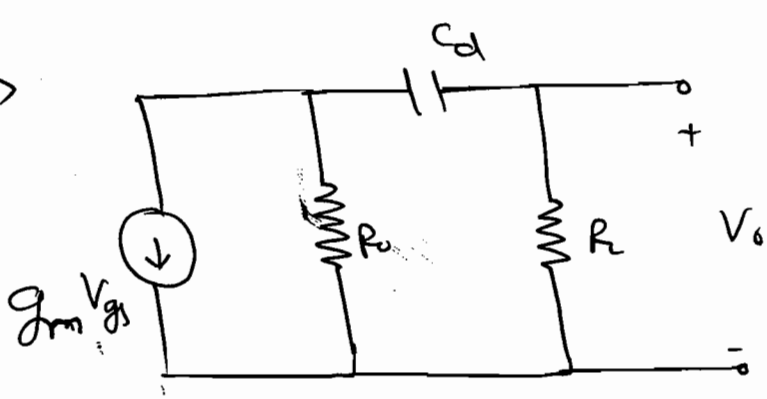
$\boxed{f_L = f_{L3}}$ (lower cut-off freq.)

i.e. due to C_d.

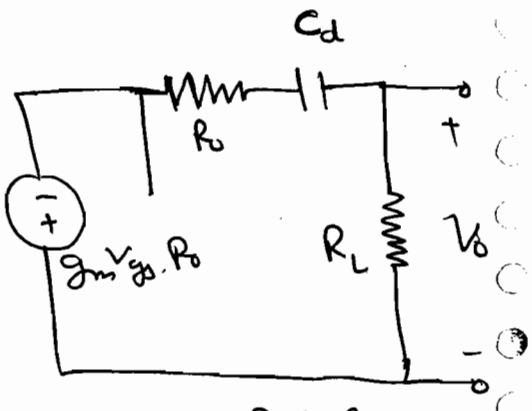
② Output side:



$\Rightarrow$

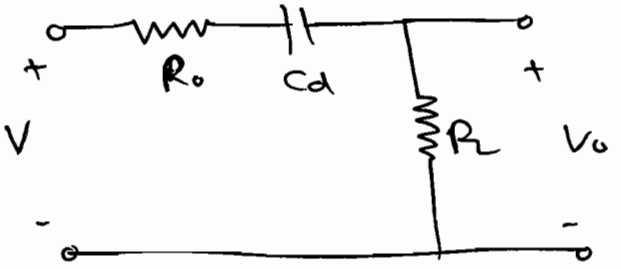


$\equiv$



$R_o = R_D \| R_d$

$\therefore$



$$\Rightarrow H(f) = \frac{R_L}{R_o + R_L + \frac{-j}{j f 2\pi C_d}}$$

$$H(f) = \frac{\frac{R_L}{R_o + R_L}}{1 + \frac{1}{j f 2\pi C_d (R_o + R_L)}}$$

$$\therefore H(f) = \frac{A_L}{1 + j\left(\frac{f_L}{f}\right)^2}$$

$$\therefore |H(f)| = \frac{A_L}{\sqrt{1 + \left(\frac{f_L}{f}\right)^2}},$$

$$\boxed{f_L = \frac{1}{2\pi C_d (R_o + R_L)}}$$

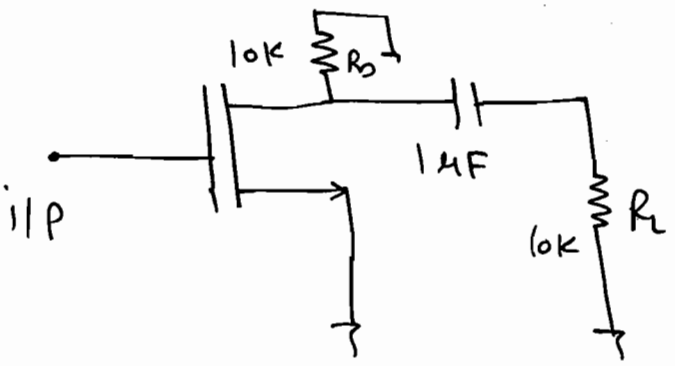
if C_s is present, then

$$\therefore \boxed{f_L = \frac{1}{2\pi C_s R_{eq}}}$$

$$R_{eq} = R_s \| \frac{1}{g_m}.$$

Q -2M

2013 ECE



find f_L?

Soln:

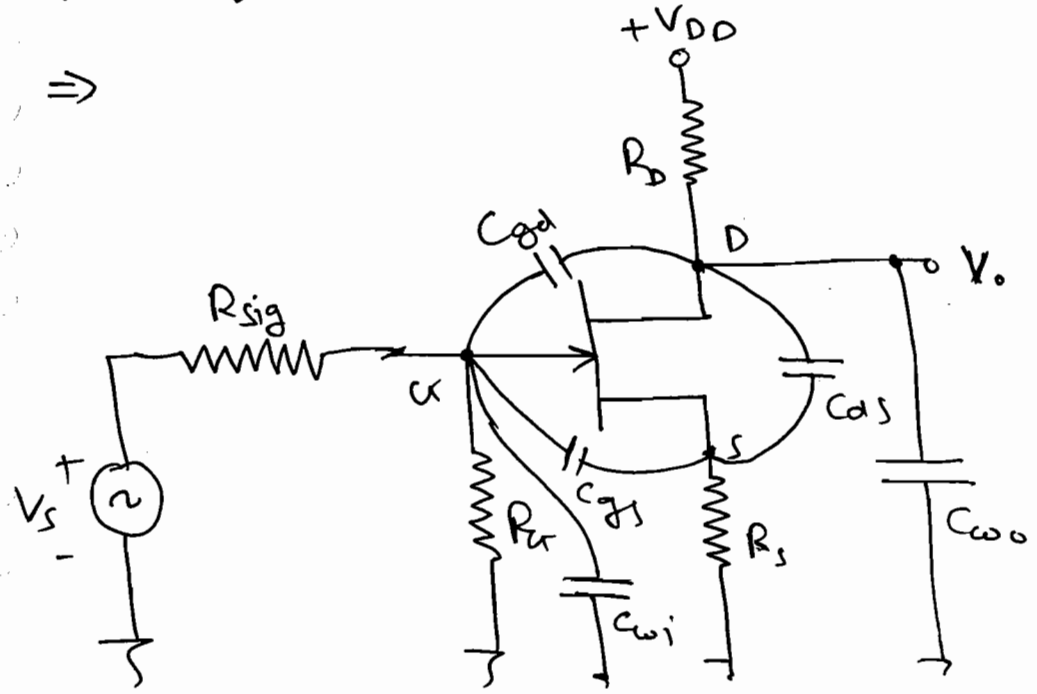
$$f_L = \frac{1}{2\pi C_d (R_D + R)} = \frac{1}{2\pi \times 10^{-6} \times 20 \times 10^3}$$

$$\therefore \boxed{f_L = 7.96\ Hz}$$

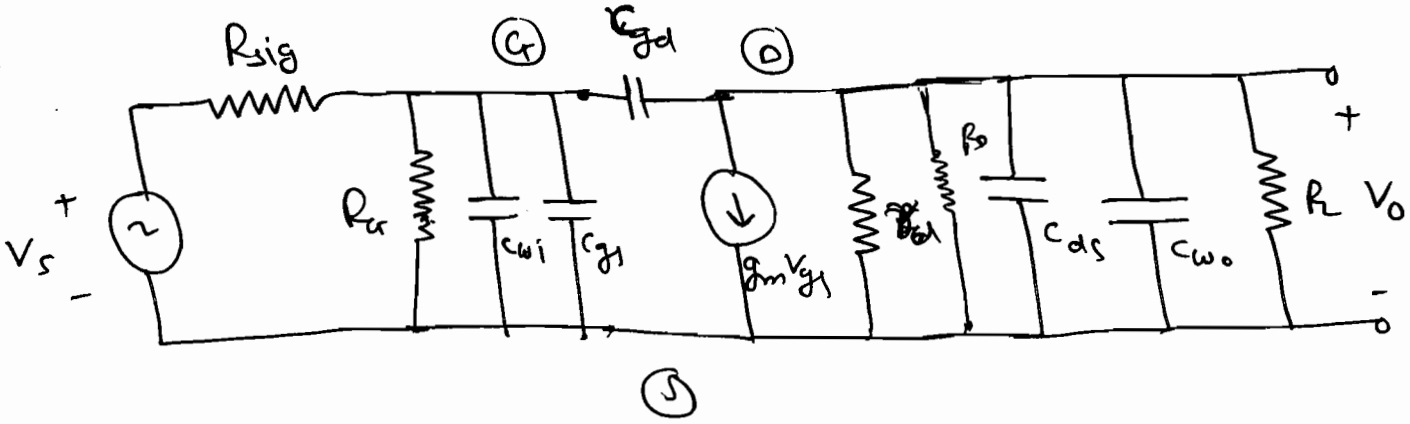
☆ High Frequency Analysis:

⇒ At Low freq. amplifier behaves like a high pass filter due to Coupling and bypass Capacitor. Therefore gain falls at low freqs. due to Coupling and bipass Cap.

⇒

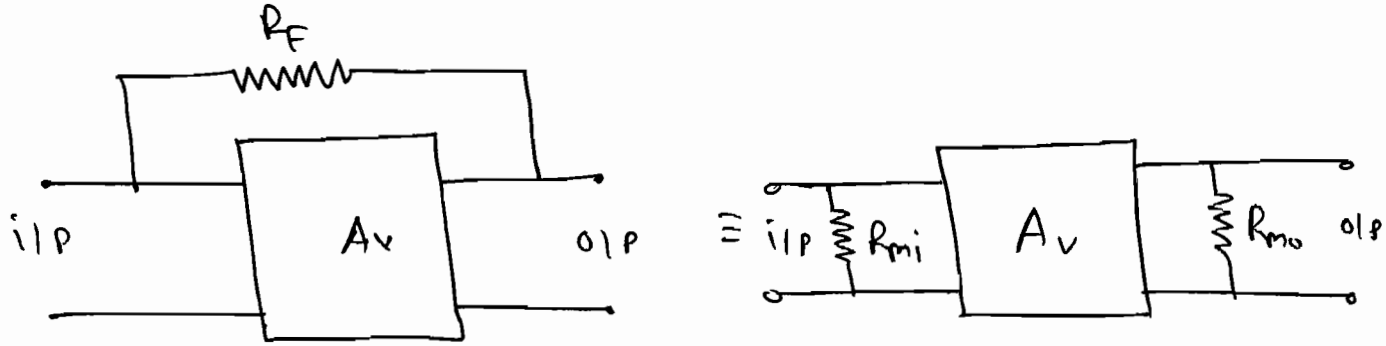


⇒ Small Signal eqn CKt:



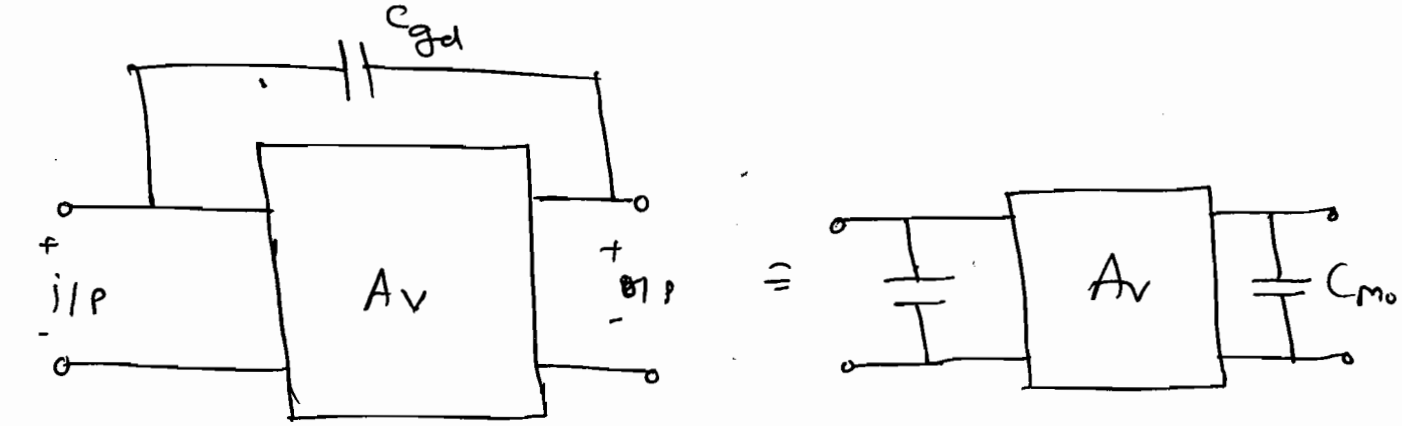
* Miller's theorem:

⇒



$$R_{mi} = \frac{R_F}{1 - A_v}, \qquad R_{mo} = \frac{R_F}{1 - \frac{1}{A_v}} \approx R_F$$ for large voltage gain.

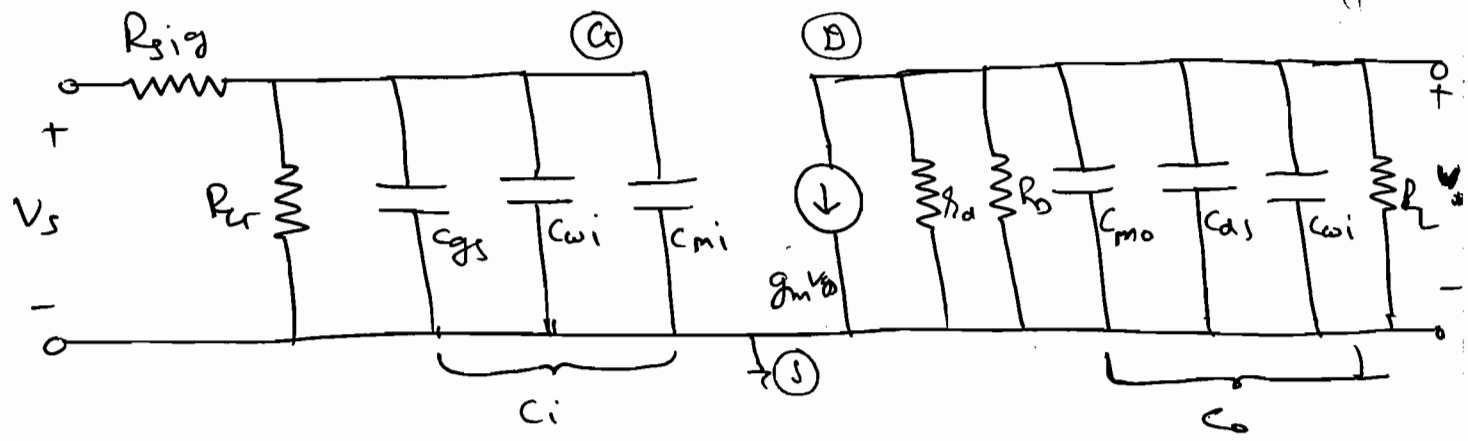
⇒



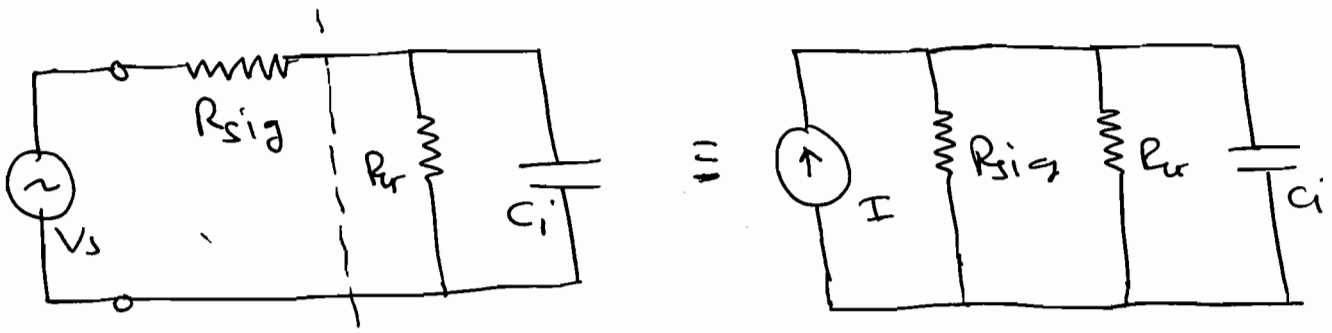
⇒ $C_{mi} = C_{gd}(1 - A_v)$.

$C_{mo} = C_{gd}\left(1 - \frac{1}{A_v}\right) \approx C_{gd}$.

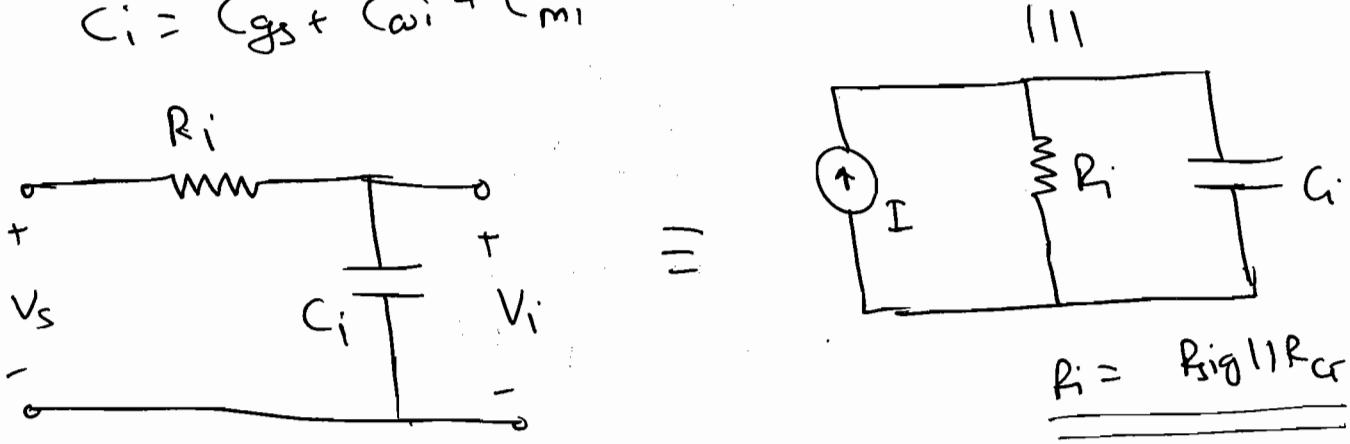
↑ for large value of A_v



① Input side:



$$C_i = C_{gs} + C_{\omega i} + C_{mi}$$



$$R_i = R_{sig} \,||\, R_G$$

$$\Rightarrow H(j\omega) = \frac{\frac{1}{j\omega C_i}}{R_i + \frac{1}{j\omega C_i}}.$$

$$H(j\omega) = \frac{1}{1 + j\omega C_i R_i}.$$

$$\therefore H(f) = \frac{1}{1 + jf2\pi C_i R_i}.$$

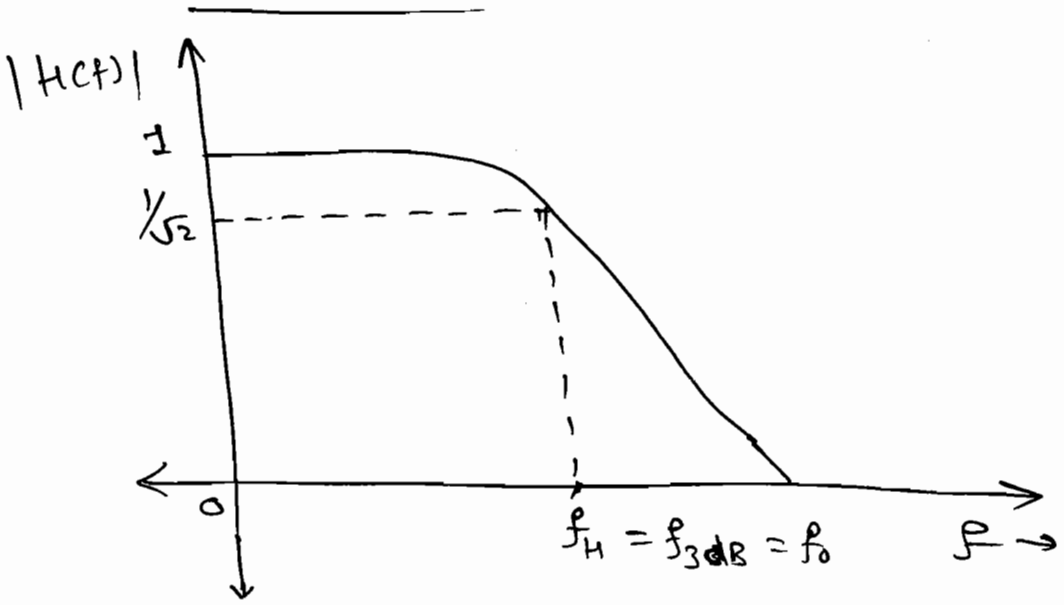
$$H(f) = \frac{1}{1 + j\frac{f}{f_H}} \Rightarrow |H(f)| = \frac{1}{\sqrt{1 + \left(\frac{f}{f_H}\right)^2}}.$$

$$\therefore \quad f_H = \frac{1}{2\pi C_i R_i}.$$

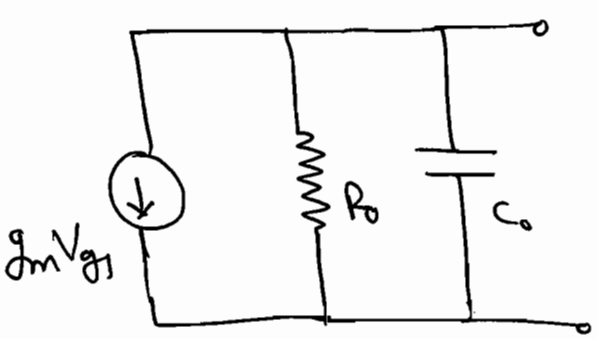
$\Rightarrow$ for $f = 0 \Rightarrow |H(f)| = 1.$

for $f = f_H \Rightarrow |H(f)| = 1/\sqrt{2}.$

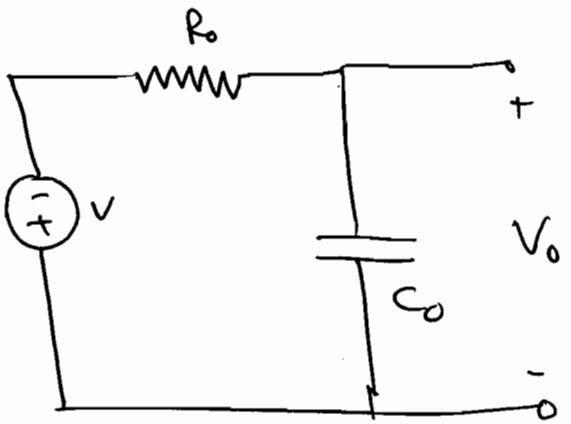
for $f = \infty \Rightarrow |H(f)| = 0.$



(2) O/P side:



$\equiv$



$$H(f) = \frac{1}{1 + jf\,2\pi C_0 R_0}.$$

$$H(f) = \frac{1}{1 + j\, f/f_H}$$

$$\therefore |H(f)| = \frac{1}{\sqrt{1 + \left(\frac{f}{f_H}\right)^2}}.$$

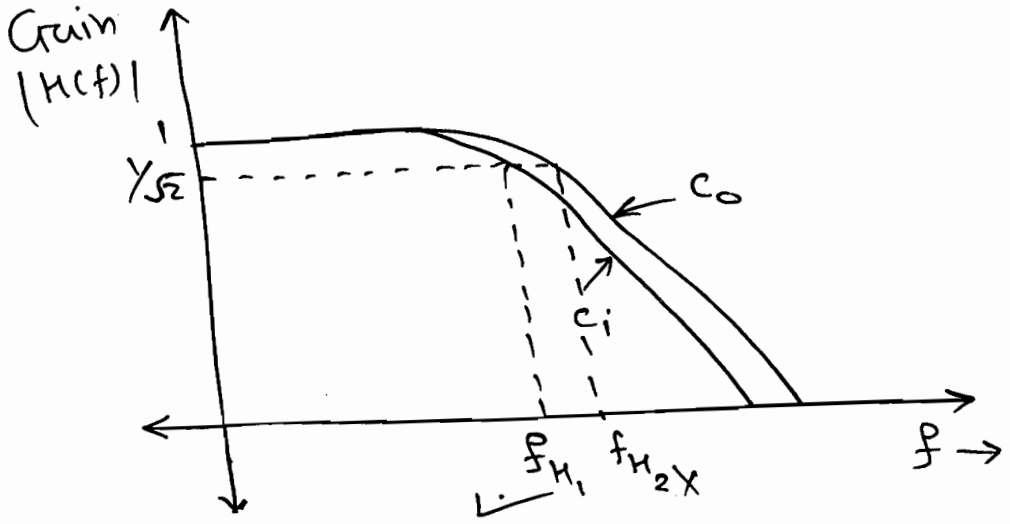
$$R_0 = R_L \| R_d \| r_0$$

$$r_0 = R_L \| R_0 \quad (\because R_0 \gg r_0)$$

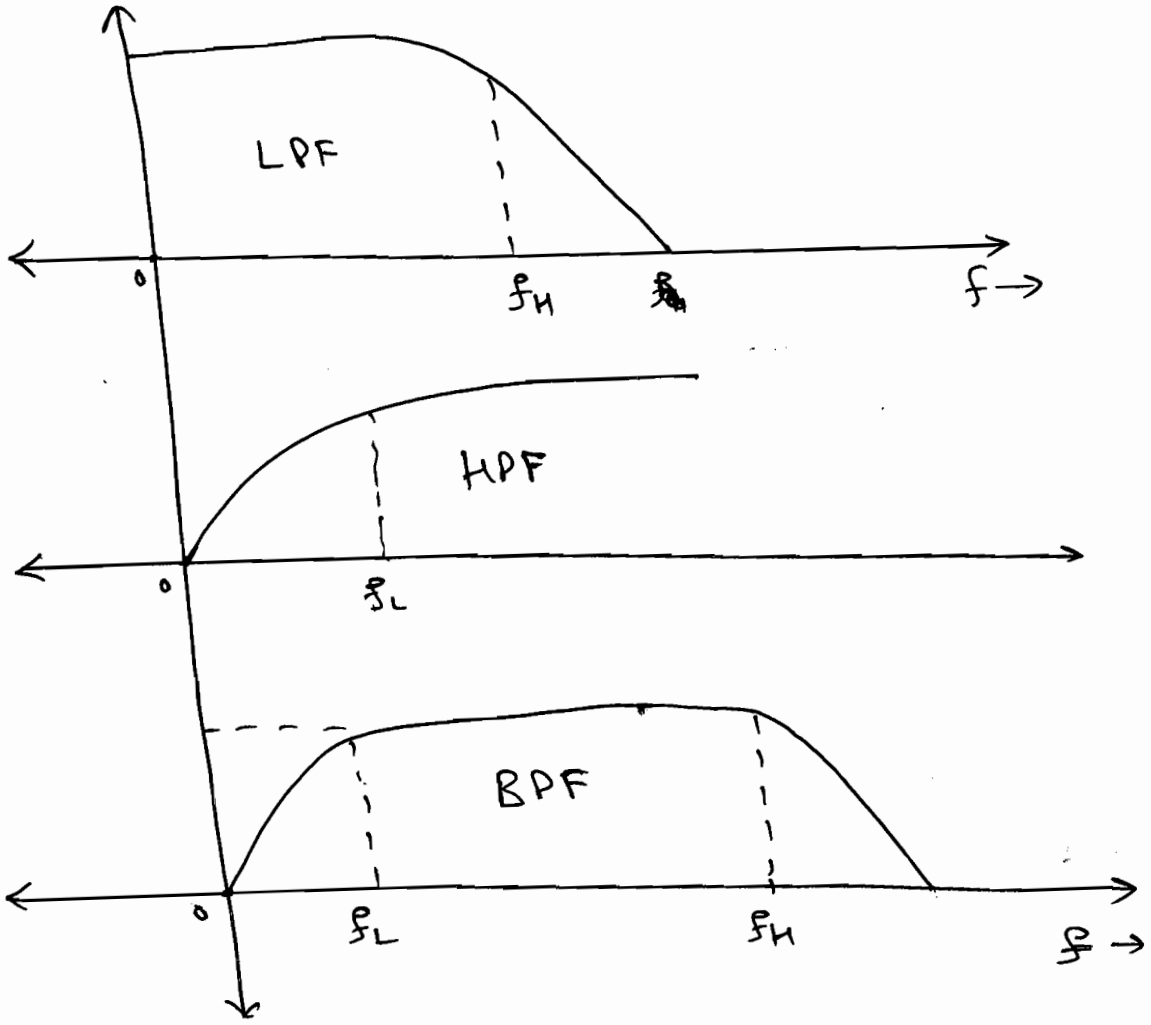
$$C_0 = C_{m0} + C_{w0} + C_{db}.$$

$$\boxed{f_H = \frac{1}{2\pi R_0 C_0}}$$

⇒



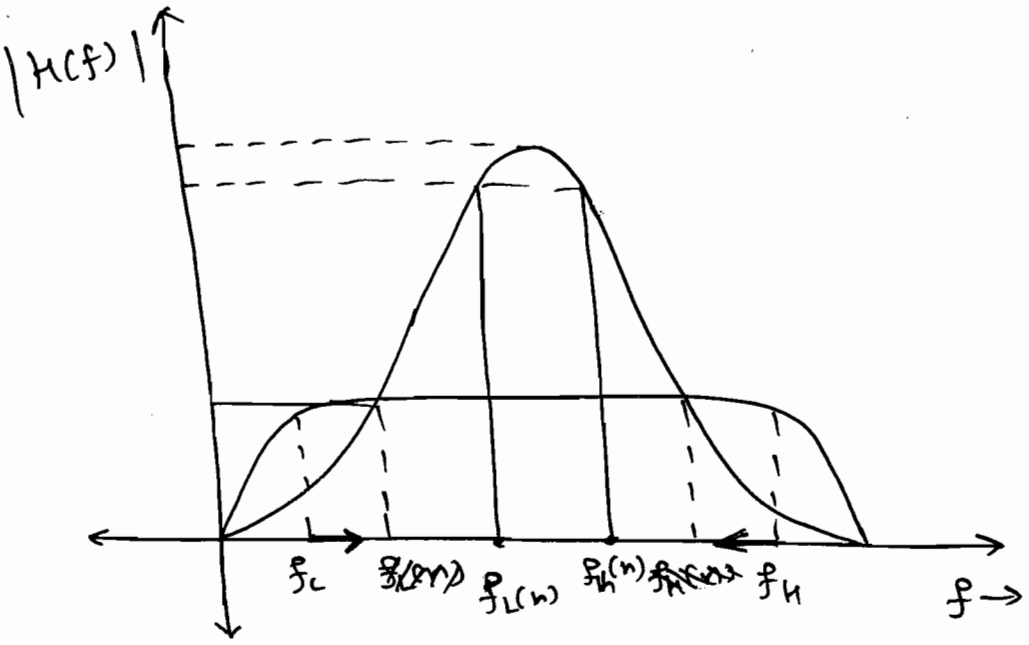
⇒



⇒ At high freq. Amp. behaves like a LPF due to junction, wiring, stray and inter-electrode capacitance. Therefore, gain falls at high frequency due to junction, wiring, stray and interelectrode capacitors.

$\Rightarrow$ Amplifier is behaving like a hpf at Low freq. and it is behaving like a LPF at high freq. Therefore, amplifier is a BPF.

$\Rightarrow$



$$BW = f_H - f_L$$

$$f_{L(n)} = \frac{f_L}{\sqrt{2^{\frac{1}{n}} - 1}}$$

$$f_{H(n)} = f_H \sqrt{2^{\frac{1}{n}} - 1}$$

$$BW(n) = f_{H(n)} - f_{L(n)}.$$

$$BW(n) = B.W. \sqrt{2^{\frac{1}{n}} - 1}$$

* Drawback of JFET:

⇒ more gate leakage current.

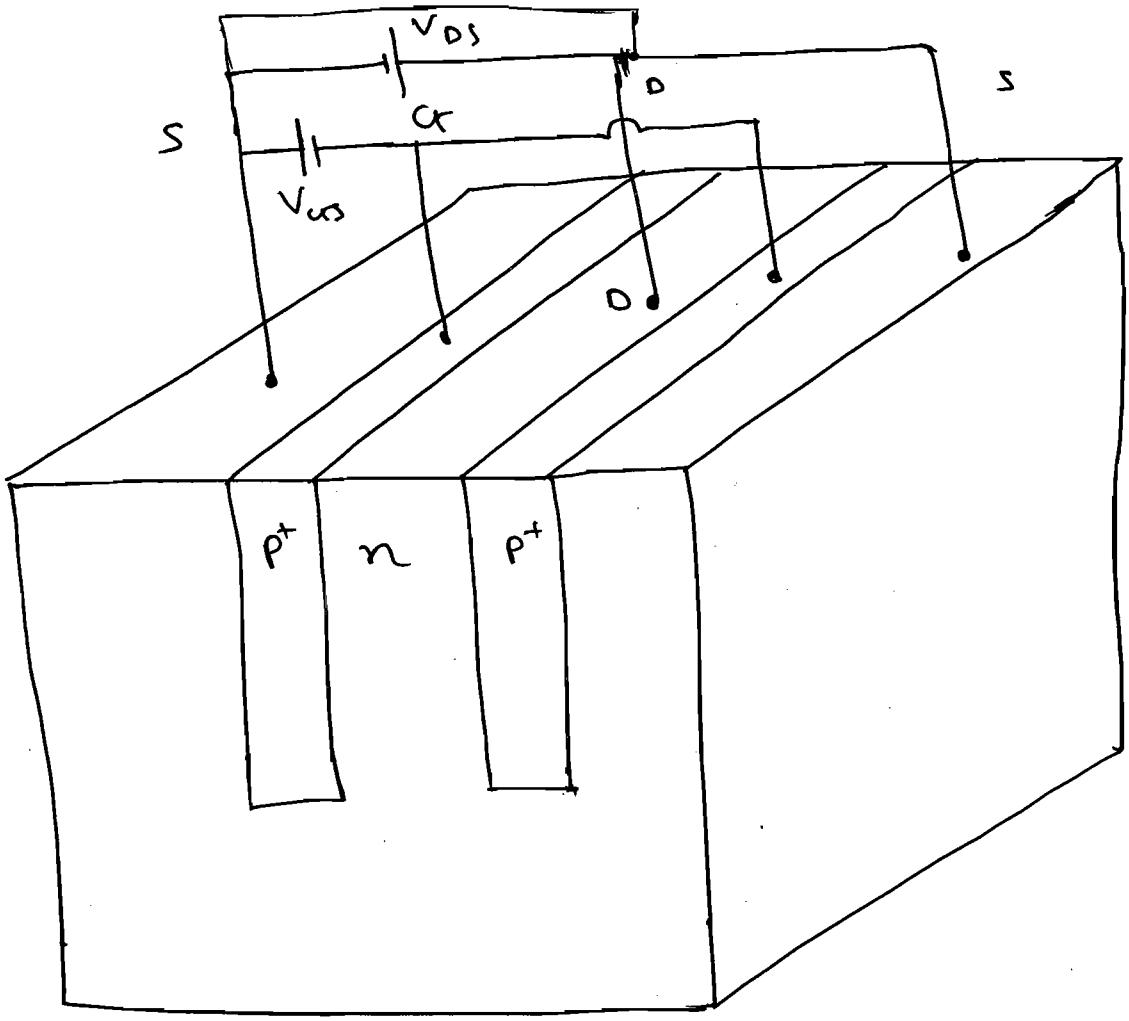
i.e. more I_{GSS}

⇒ large size.

⇒ V_{DS} & V_{GS} have different polarities.

	n-JFET	p-JFET
V_{DS} :	+ve	V_{DS} = -ve
V_{GS} :	-ve	V_{GS} = +ve.

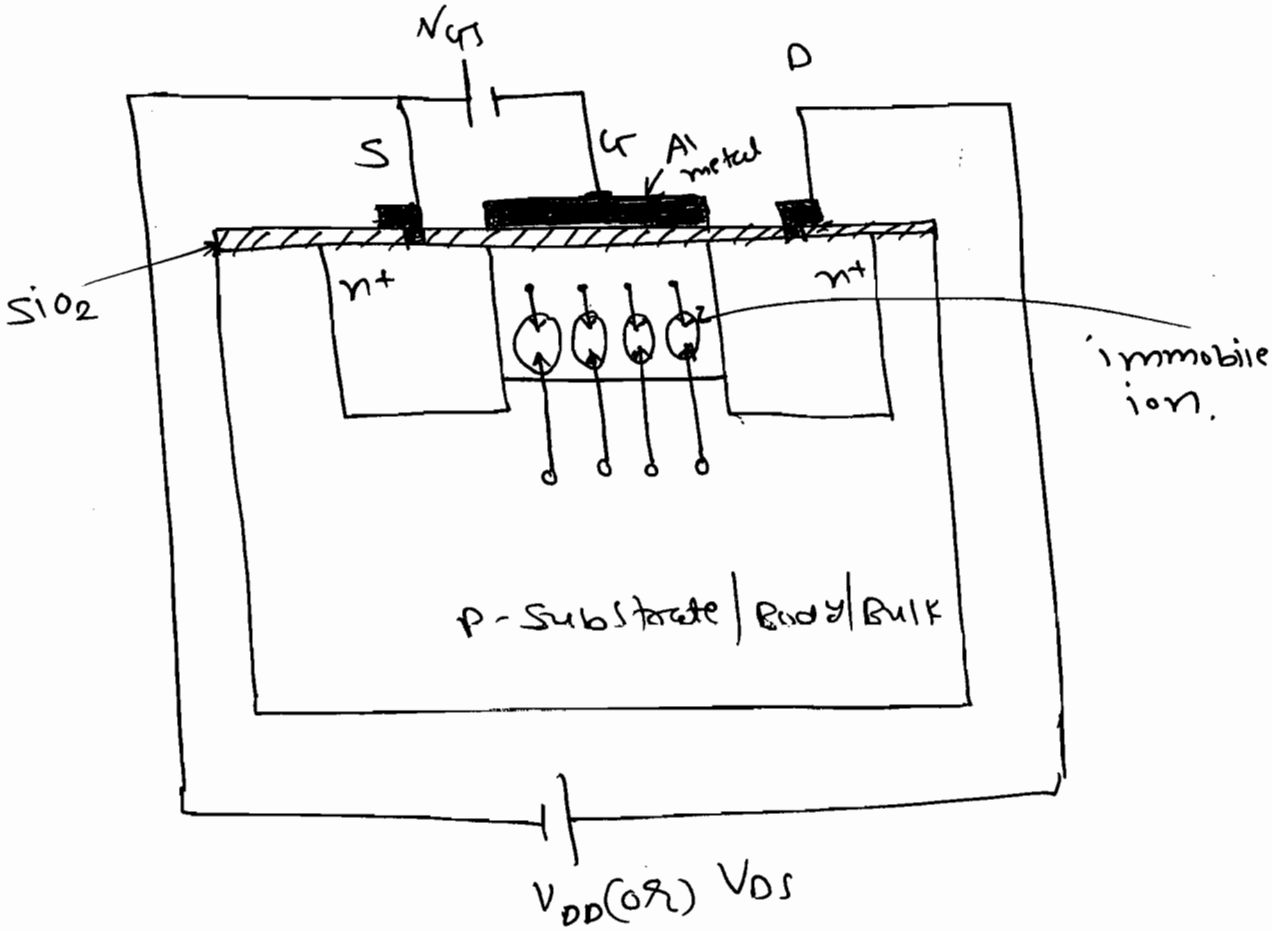
⇒ Now a days following Const^n of FET is used.



☆ Depletion MOSFET :-

① n- Channel Depletion MOSFET: (n- D MOSFET)

⇒

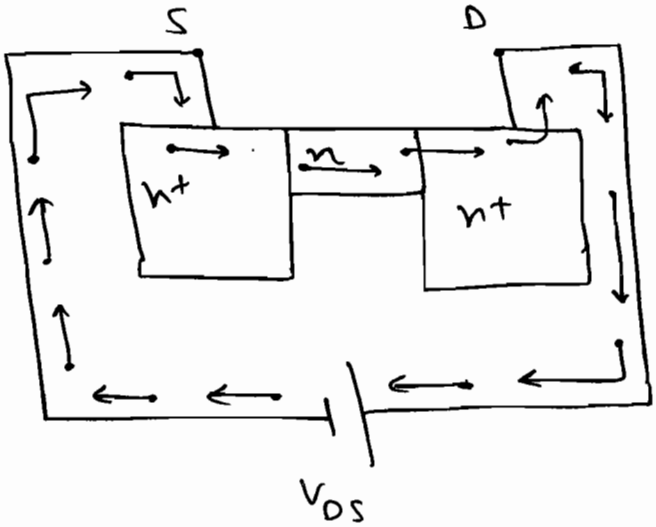


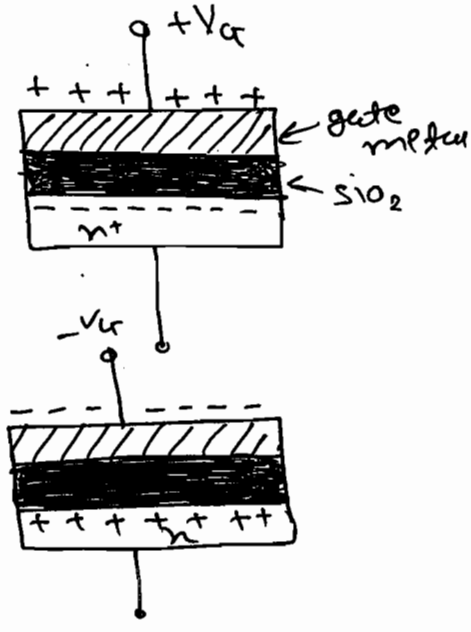
⇒ $R_{i\,BJT} < R_{i\,JFET}$

$R_{i\,JFET} < R_{i\,MOSFET}$

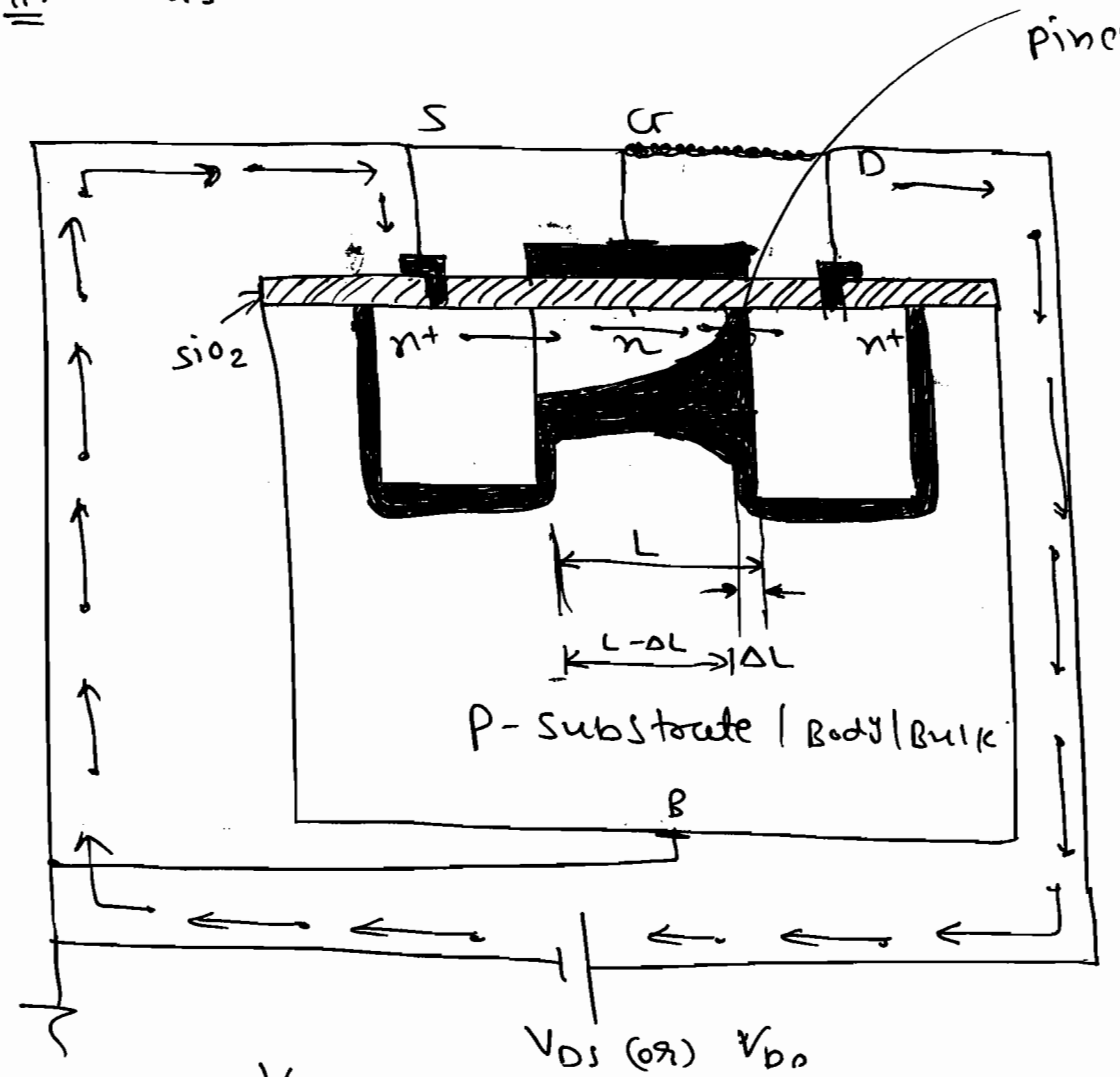
$\therefore$ $R_{i\,BJT} < R_{i\,JFET} < R_{i\,MOSFET}$.

⇒

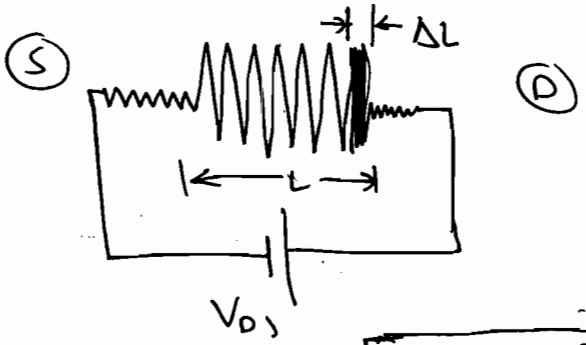




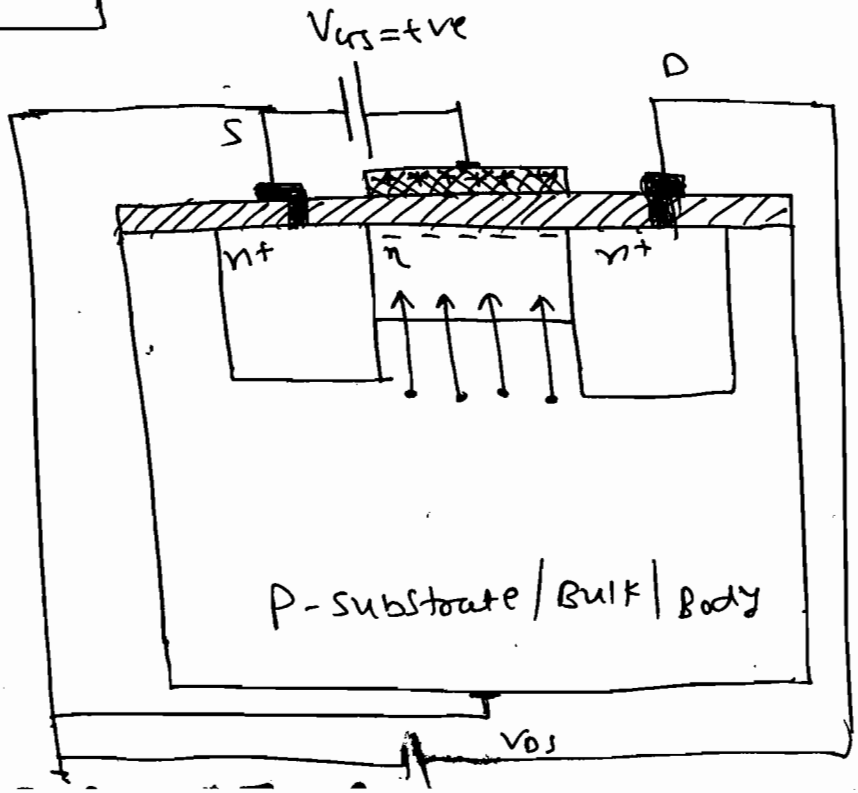
Case-(i): $V_{GS} = 0$.



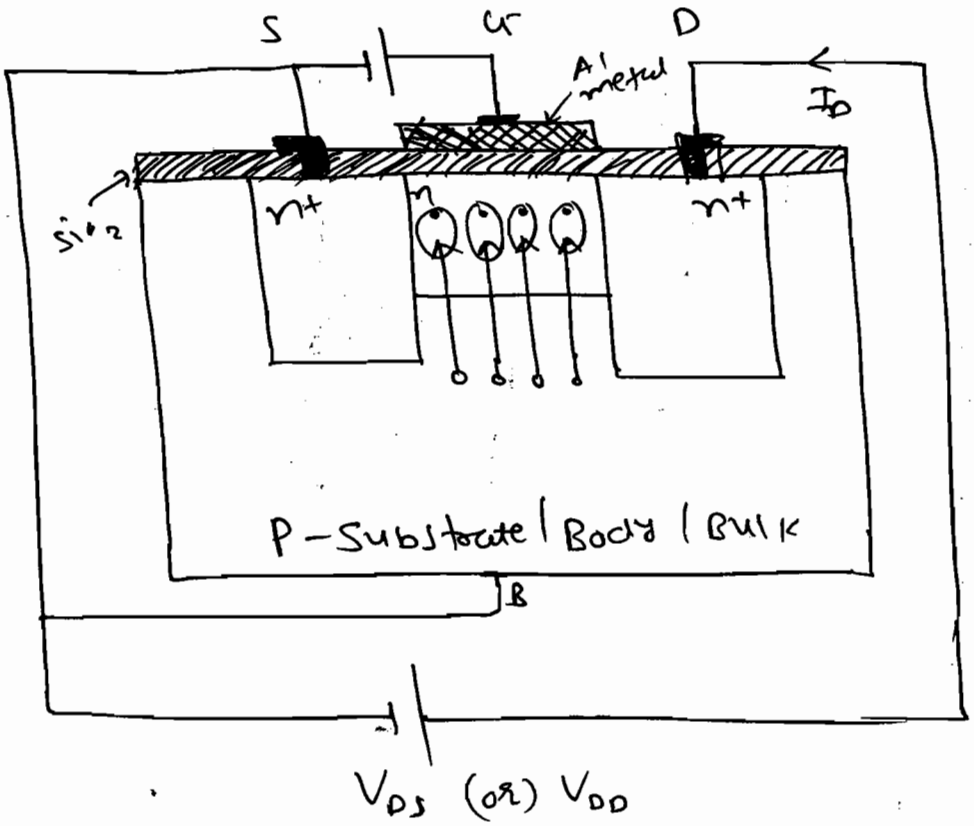
$$E = \frac{V_{DS}}{L}$$



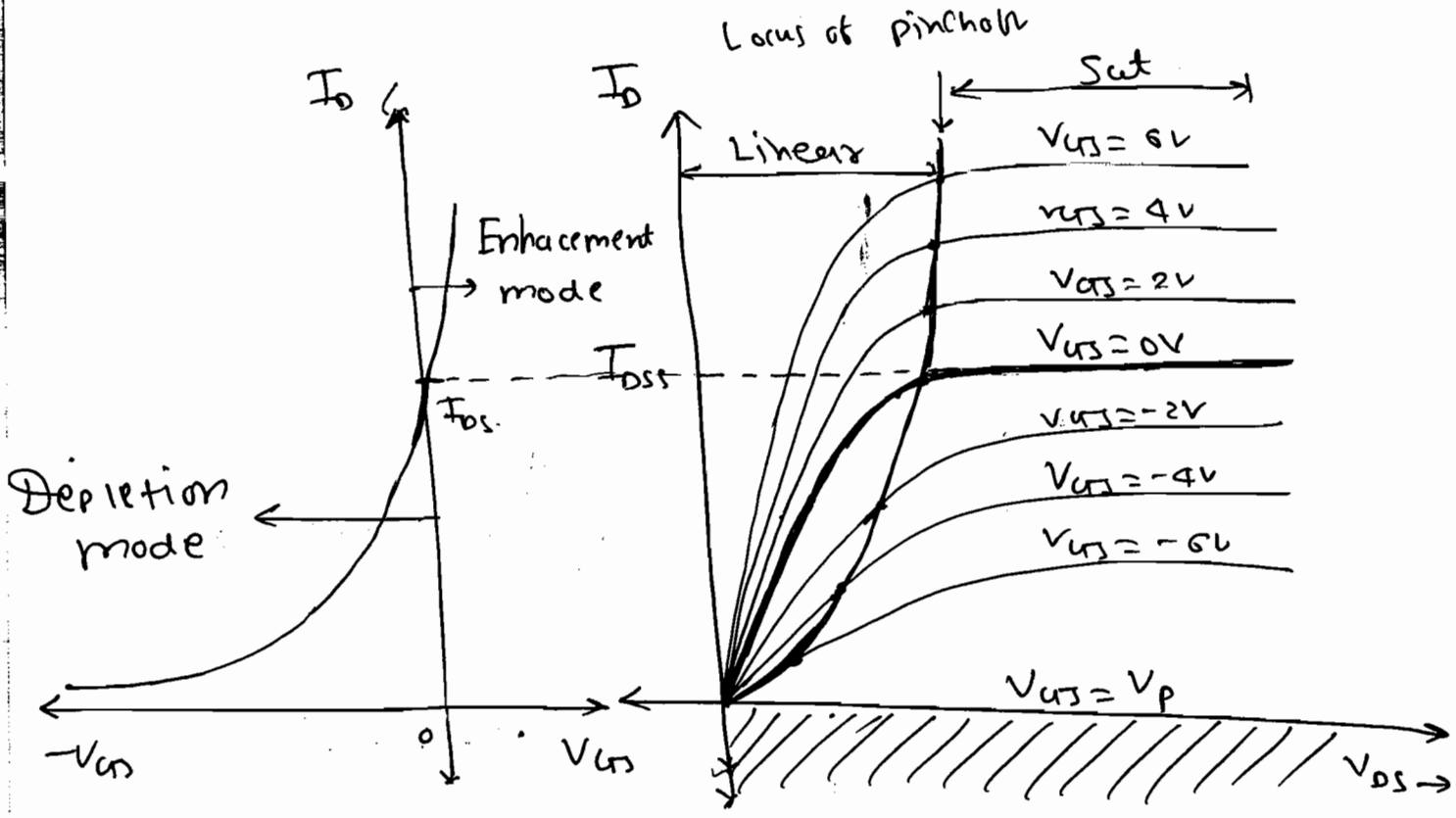
Case-(ii) $V_{GS} = +ve$.



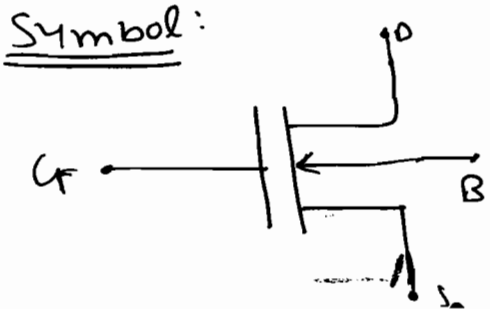
Case-(iii) V_{GS} = -ve



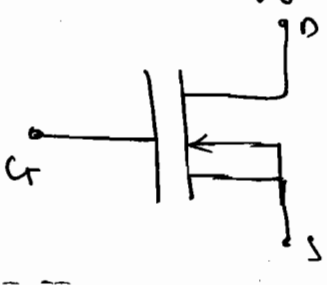
* Drain and Transfer Characteristics:



* Symbol:



(or)



⇒ Important points to be remember:

⇒ Pinch-off Voltage is -ve for n-channel DMOSFET.

⇒ n-channel Depletion MOSFET operates in enhancement mode for $+V_{GS}$ value and it operates in depletion mode for -ve V_{GS} value.

⇒ Depletion MOS-FET operates in depletion and enhancement mode.

⇒ In descrete n-Channel DMOSFET Substrate (or) Body (or) Bulk is connected to the ground (or) Source terminal. where as in IC's it Should be connected to Most -ve voltage.

⇒ n-channel depletion MOSFET will be on for +ve V_{GS} value and it will be OFF for -ve V_{GS} value (i.e. $V_{GS} \leq V_p$).

⇒ Condition for pinch-off (or) ~~Boundary~~ Sat. is

$$V_{DS} = V_{GS} - V_p.$$

(V_{DS}: +ve; V_{GS}: +ve (or) -ve; V_p: -ve)

⇒ Transfer characteristics of a depletion MOSFET gives pinch-off Voltage (V_P), I_{DSS} and transconductance g_m.

⇒ For $V_{GS} \leq V_P$ operates in Cut-off region and its drain current $I_D = 0$.

⇒ For $V_{DS} < V_{GS} - V_P$ it operates in linear region and its drain current

$$I_D = K_n \left[2 (V_{GS} - V_P) V_{DS} - V_{DS}^2 \right]$$

K_n = Constant $= \frac{I_{DSS}}{V_P^2}$ A/V^2.

$$\therefore \boxed{I_D = \frac{2 I_{DSS}}{V_P^2} \left[(V_{GS} - V_P) V_{DS} - \frac{1}{2} V_{DSS}^2 \right].}$$

(V_{GS}: +ve or -ve; V_P: -ve; V_{DS}: +ve)

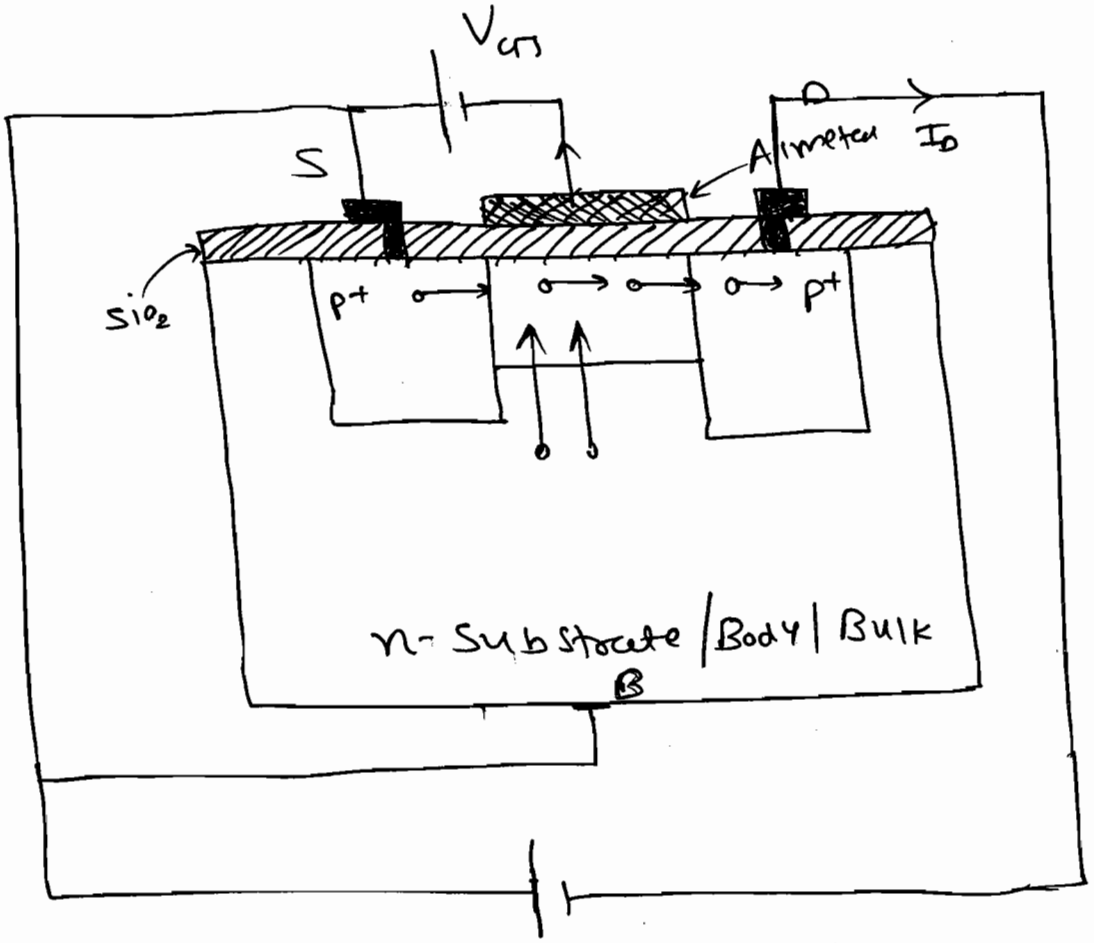
⇒ for $V_{DS} \geq (V_{GS} - V_P)$ it operates in Saturation region and its drain current

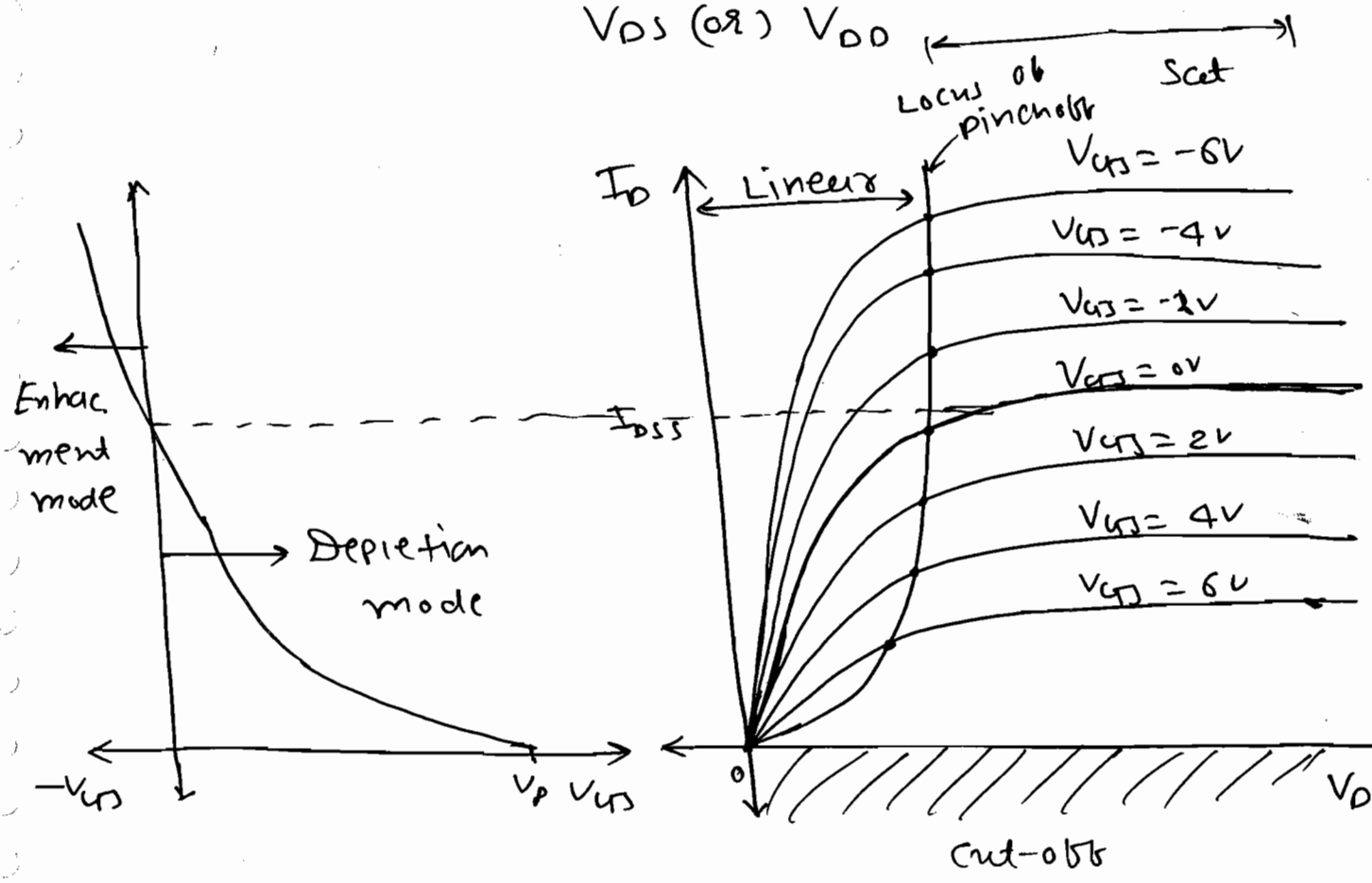
$$I_D = K_n \left[V_{GS} - V_P \right]^2, \quad K_n = \frac{I_{DSS}}{V_P^2} \ A/V^2$$

$$\therefore \boxed{I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_P} \right]^2}$$

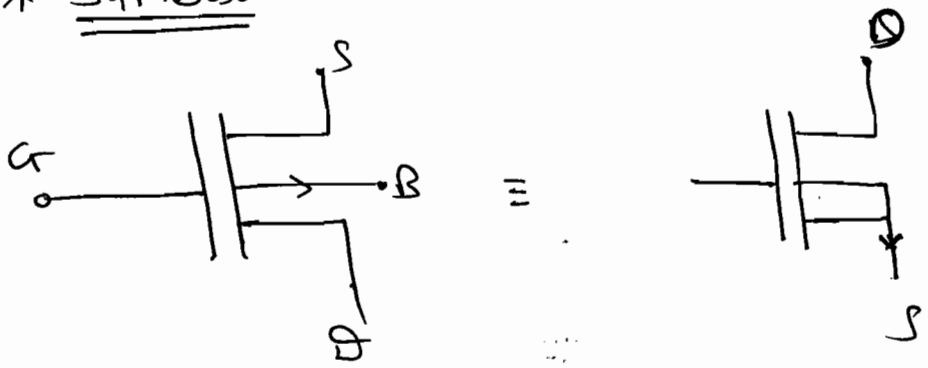
(V_{GS}: +ve or -ve; V_P: -ve.)

☆ P-Channel Depletion MOSFET:





* Symbol:



* Imp. points to be remember:

⇒ P-Channel depletion MOSFET operates with +ve as well as -ve V_{GS} value.

⇒ pinch-off Voltage is +ve for P-DMOSFET

⇒ P-Channel depletion MOSFET operates in depletion mode for $+V_{GS}$ and it operates in enhancement mode for $-V_{GS}$ value.

⇒ In descrete P-DMOSFET Substrate (or) Body (or) Bulk should be connected to the ground (or) source terminal. whereas in Ic's it should be connected to the most +ve Voltage.

⇒ P-DMOSFET will be ON for -ve V_{GS} values and it will be OFF for +ve values (i.e. $V_{GS} \geq V_P$).

⇒ Condition for pinch-off (or) Saturation

$$-ve \rightarrow V_{DS} = \underset{\uparrow}{V_{GS} - V_P} \leftarrow +ve$$

+ve or ±ve

⇒ For $V_{GS} \geq V_P$ P-DMOSFET operates in cut-off region and its drain current $I_D = 0$.

⇒ For $V_{DS} > V_{GS} - V_P$ it operates in linear region and it drain current is given by,

$$I_D = k_p \left[2(V_{GS} - V_P) V_{DS} - V_{DS}^2 \right].$$

$$k_p = \frac{I_{DSS}}{V_P^2}.$$

$$\therefore \boxed{I_D = \frac{2 I_{DSS}}{V_P^2} \left[(V_{GS} - V_P) V_{DS} - \frac{1}{2} V_{DS}^2 \right].}$$

(V_{GS}: +ve (or) -ve; V_P: + ve; V_{DS}: +ve)

⇒ $V_{DS} \leq V_{GS} - V_P$ it operates in Saturation region and drain current,

$$I_D = k_p \left[V_{GS} - V_P \right]^2.$$

$$\therefore I_D = \frac{I_{DSS}}{V_P^2} \left[V_{GS} - V_P \right]^2.$$

$$\therefore \boxed{I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_P} \right]^2.}$$

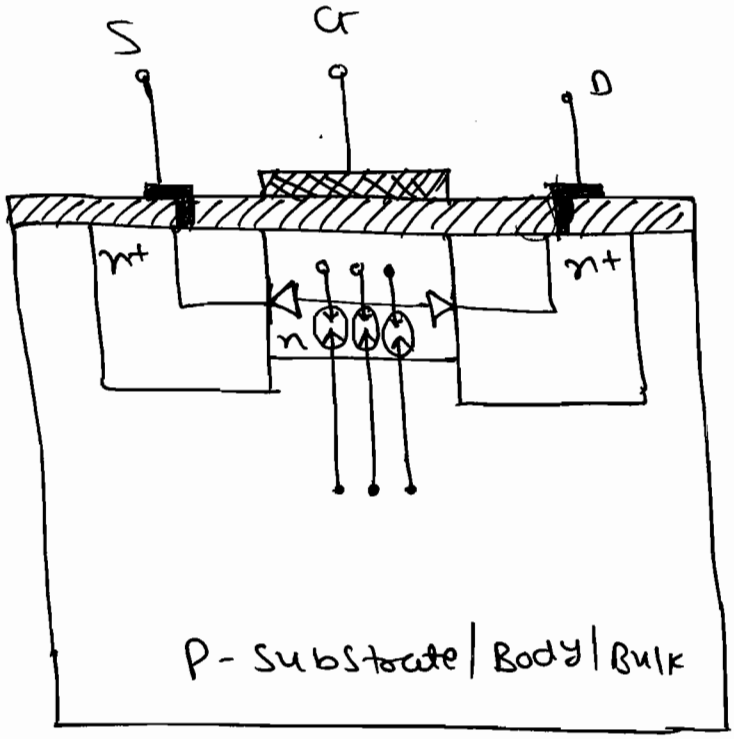
(V_{GS}: +ve (or) -ve; V_P: +ve.)

⇒ We prefere D-MOSFET for resistor instead of E-MOSFET.

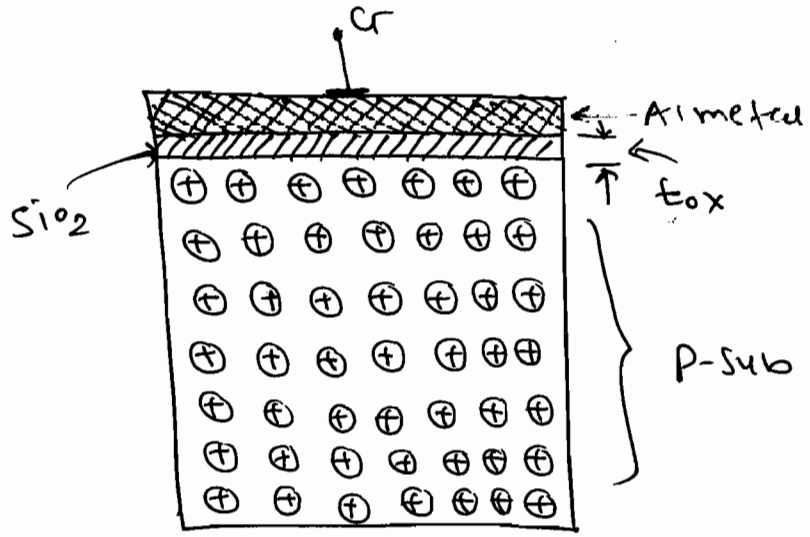
✡ Enhancement MOSFET:

① n- channel enhancement MOSFET: (n- EMOSFET)

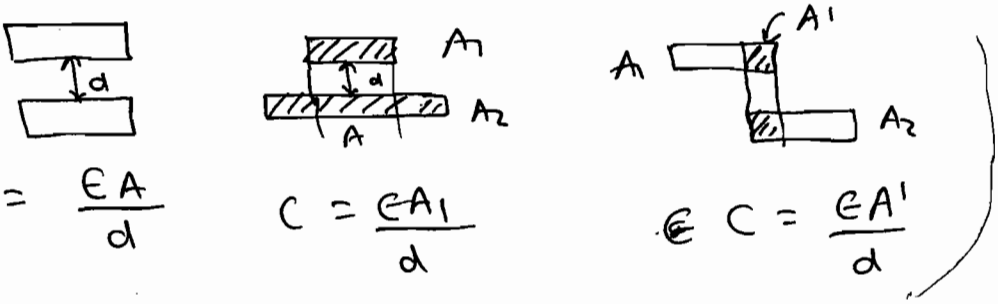
⇒



*



⇒



$C = \frac{\epsilon A}{d}$ $\quad C = \frac{\epsilon A_1}{d}$ $\quad \epsilon\, C = \frac{\epsilon A'}{d}$

$\Rightarrow \frac{C}{A} = \epsilon / d$ F/cm² (or) F/m².

$\therefore \frac{C}{A} = \epsilon/d$ F/cm² (or) F/m².

A = Common Area bet^n two plate.

$\therefore C_{ox}$ = oxide Capacitor per unit area

$\therefore C_{ox} = \frac{\epsilon}{t_{ox}}$.

$\therefore \boxed{C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}}$ F/cm² (or) F/m².

$\Rightarrow t_{ox}$: Gate oxide thickness

ϵ_{ox} : permitivity of SiO_2

ϵ_{ox} : $\epsilon_{rox} \cdot \epsilon_0$, ϵ_{rox} = relative permitivity of SiO_2

$= 3.9 \approx 4$

$\epsilon_0 = 8.85 \times 10^{-12}$ F/m

$\epsilon_0 = 8.85 \times 10^{-14}$ F/cm.

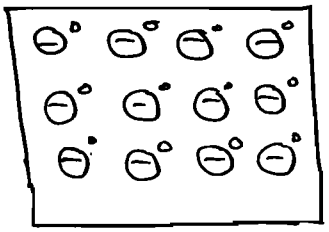
$\therefore C_0 = C_{ox} \cdot A$

$\therefore \boxed{C_0 = C_{ox} \times WL}$ (F)

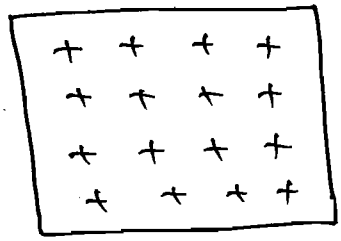
$\therefore C_0$ = oxide Capacitance.

* P-type representation:

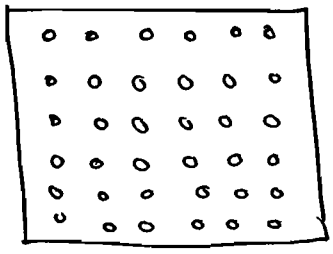
$\Rightarrow$



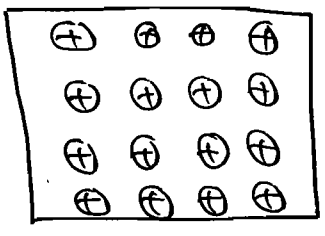
EDC



EDC



EDC

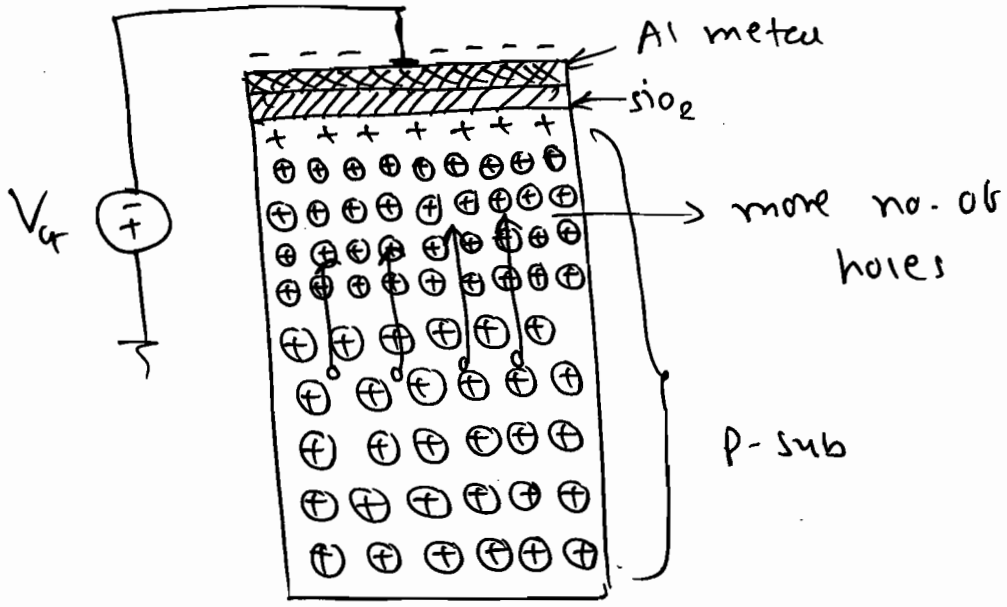


⊕ : hole

⊖ : electron

VLSI

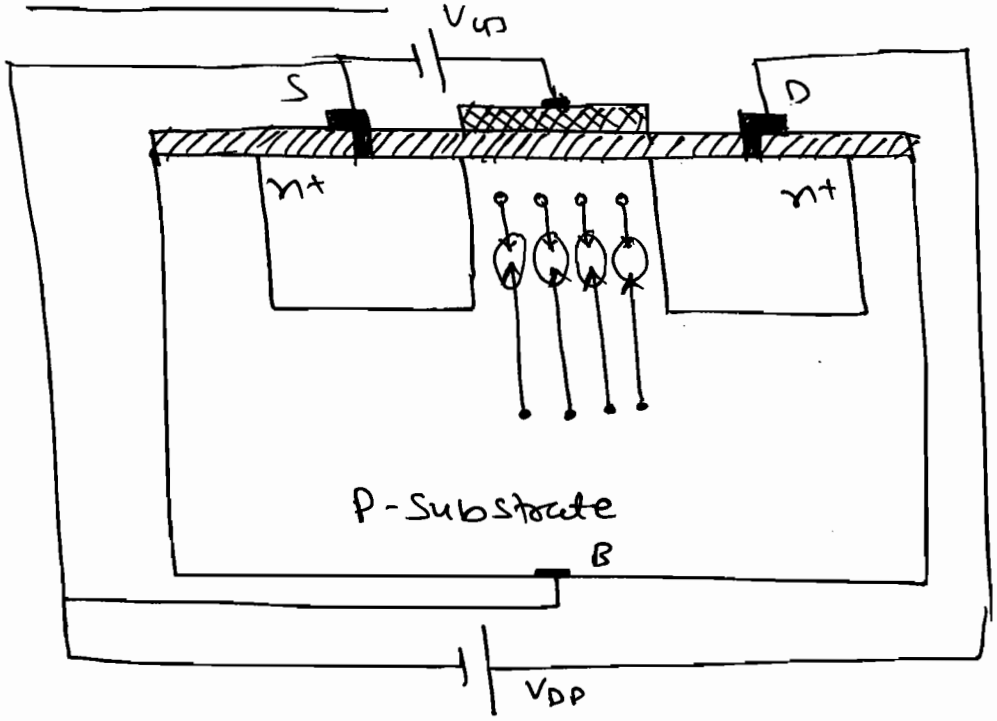
$\Rightarrow$ $V_{GB} = -Ve$

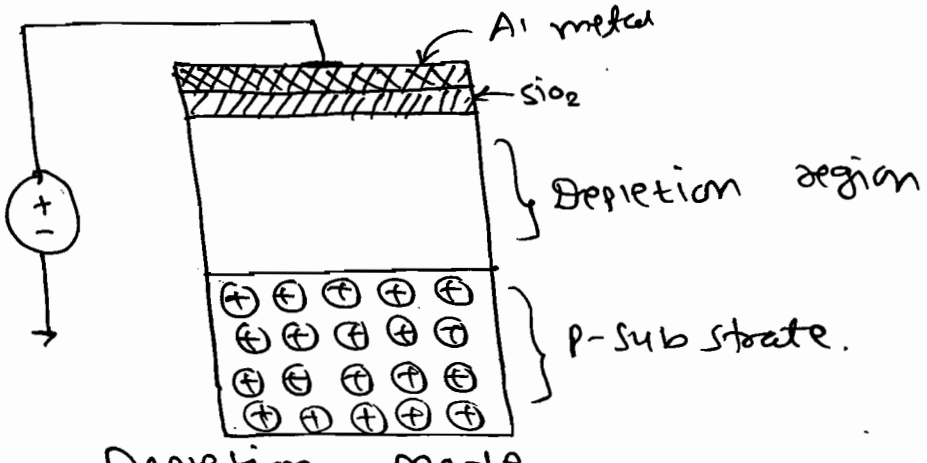


Accumulation mode.

C_{ox} is same as that of for $V_{GS} = 0V$.

$\Rightarrow$ $0 < V_{GS} < V_T$:





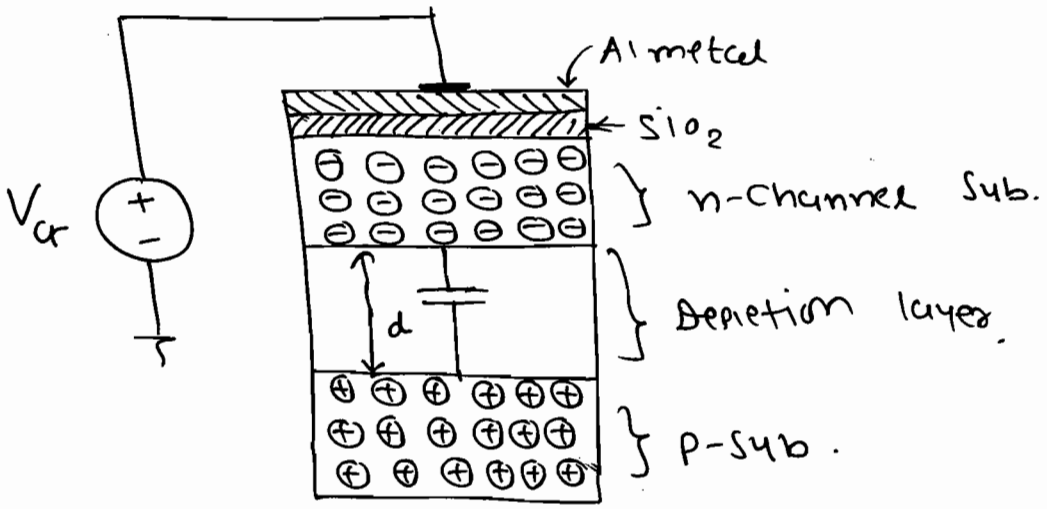
$\cdot C_{ox} = \frac{\epsilon A}{d}$

$C_{ox} \downarrow$ because $d \uparrow$

Depletion mode.

③ $V_G > V_T$.

⇒



(Inversion mode).

⇒ ~~$C_{ox} =$~~ $\frac{\epsilon_{ox}}{t_{ox}}$

C_{dep} : depletion Capacitance per unit area

$C_{dep} = \frac{\epsilon_{si} \cdot A}{d}$ F/cm² (or) F/m².

ϵ_{si} : Permitivity of silicon Si.

d : Depletion layer thickness.

ϵ_{si} : $\epsilon_{rsi} \cdot \epsilon_0$, $\epsilon_{rsi} = 11.7 \approx 12$

$\epsilon_0 = 8.85 \times 10^{-12}$ F/m.

⇒ $C_d = C_{dep} \cdot A = C_{dep} \cdot W \times L$.

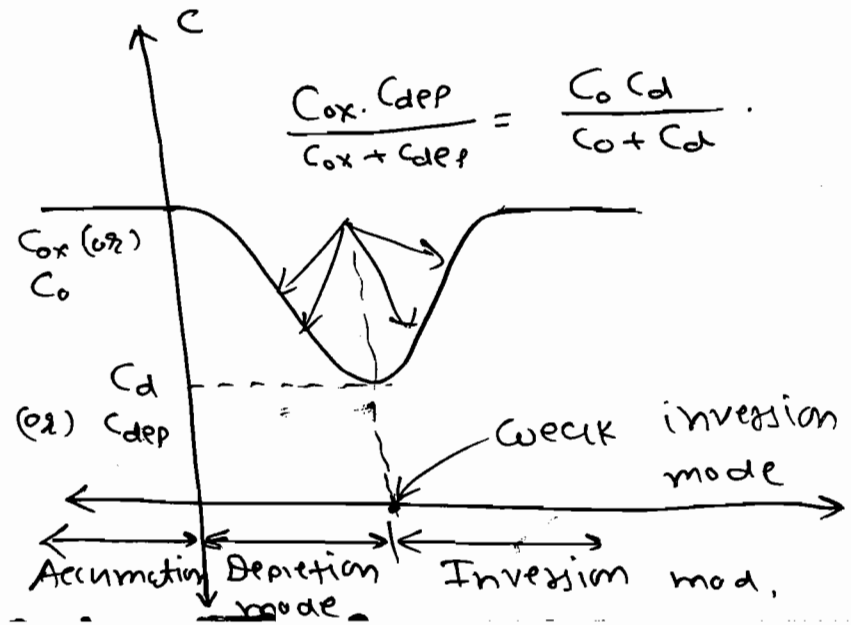
C_d : depletion Capacitance.

⇒ $C_{eq} = \frac{C_{ox} \cdot C_{dep}}{C_{ox} + C_{dep}}$.

$\therefore C_{eq} = \frac{C_o \cdot C_d}{C_o + C_d}$.

⇒ If $t_{ox} << d$. Imp.

⇒ $\boxed{\begin{array}{l} C_{ox} >> C_{dep} \\ C_o >> C_d \end{array}}$



Q-22
CRO
Page-48:

Here, $C_o = 7\,PF$

$\therefore C_o = \frac{\epsilon_{ox} \cdot A}{t_{ox}}$.

$\therefore t_{ox} = \frac{3.5 \times 10^{-13} \times 10^{-4}}{7 \times 10^{-12}}$

$t_{ox} = 0.5 \times 10^{-5}\ cm$

$\therefore t_{ox} = 0.5 \times 10^{-5} \times 10^{-2}$.

$\boxed{t_{ox} = 50nm}$

$\Rightarrow C_{eq} = \frac{C_d \cdot C_{ox}}{C_d + C_{ox}}$

$C_d = \frac{\epsilon_{si} \cdot A}{d}$.

$\therefore 1 = \frac{C_d \times 7}{C_d + 7}$.

$\therefore C_d + 7 = 7C_d$.

$\therefore C_d = 1.16\,PF$.

$\therefore d = \frac{1 \times 10^{-12} \times 10^{-4}}{1 \times 10^{-12}} \times 6$

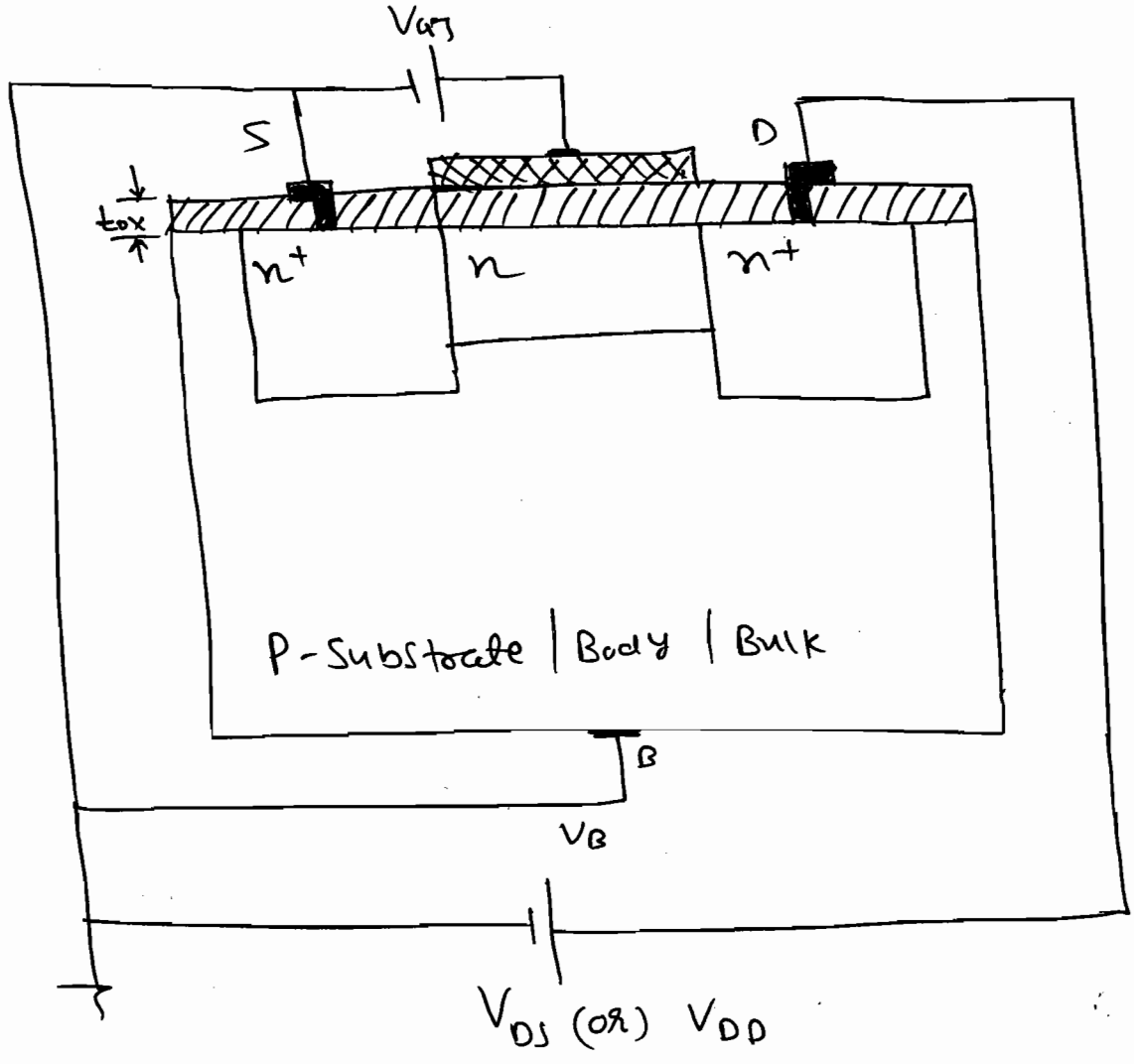
$\therefore d = 0.143 \times 10^{-4}\ cm$

$\therefore \boxed{d = 0.143\mu m.}$

* Threshold Voltage: (V_T):

⇒ Threshold voltage is the minimum gate to source voltage required to accumulate sufficient no. of carriers and to form a channel bet^n source and drain under the gate.

⇒



⇒ t_{ox} : Gate oxide thickness.

V_{SB} : Source to body voltage.

N_A (OR) N_D : Substrate doping density (OR) Concentration.

⇒ Threshold Voltage depends on

- Gate oxide thickness (t_{ox}).
- Source to body voltage (V_{SB}).
- Substrate doping density (OR) Concentration (N_A OR N_D).

→ $\boxed{V_T : f(t_{ox}, V_{SB}, N_A \text{ (OR) } N_D).}$

⇒ Threshold Voltage of a MOSFET increases as gate oxide thickness

increases (or) it decreases as t_{ox} decreases.

→ $t_{ox} \uparrow \rightarrow V_T \uparrow$

$t_{ox} \downarrow \rightarrow V_T \downarrow$.

⇒ Threshold voltage of a MOSFET is decreases as source to Body voltage decreases (or) it increases with increas in V_{SB}.

⇒ $V_{SB} \uparrow \rightarrow V_T \uparrow$

$V_{SB} \downarrow \rightarrow V_T \downarrow$.

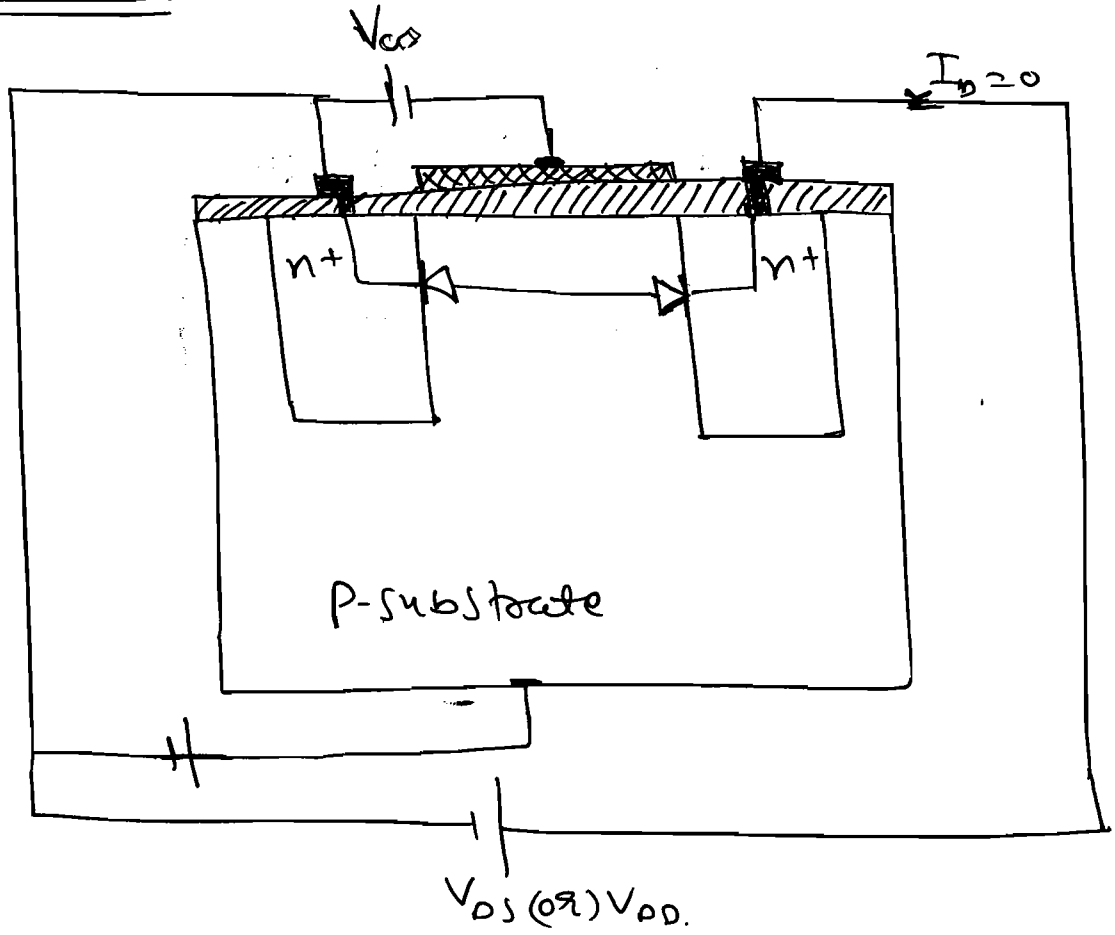
⇒ Threshold voltage of a MOSFET increases as increases in doping density increases. (or) it decreases as substrate dopping density decreases.

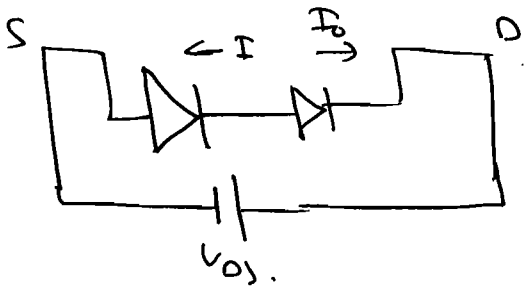
N_A (or) $N_D \uparrow \rightarrow V_T \uparrow$

N_A (or) $N_D \downarrow \rightarrow V_T \downarrow$.

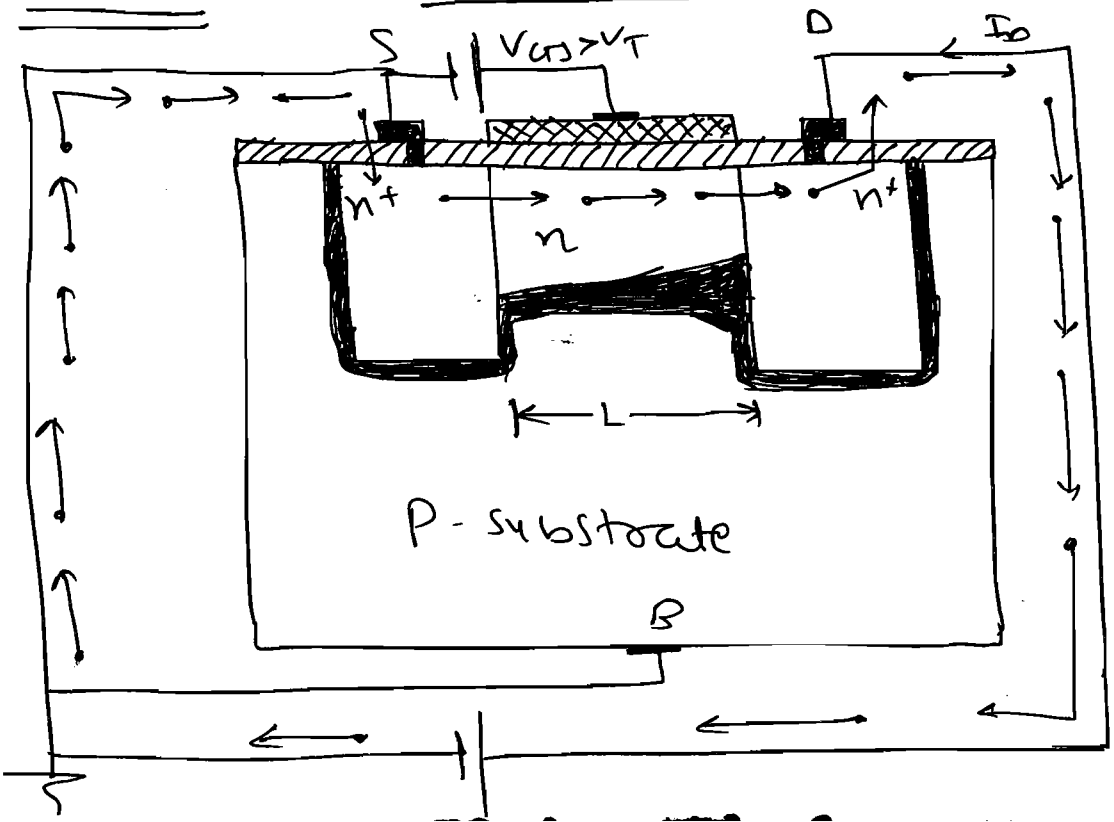
⇒ Threshold voltage is +ve for n-channel enhancement MOSFET and it is -ve for p- channel.

(i) $V_{GS} < V_T$: (cut-off).

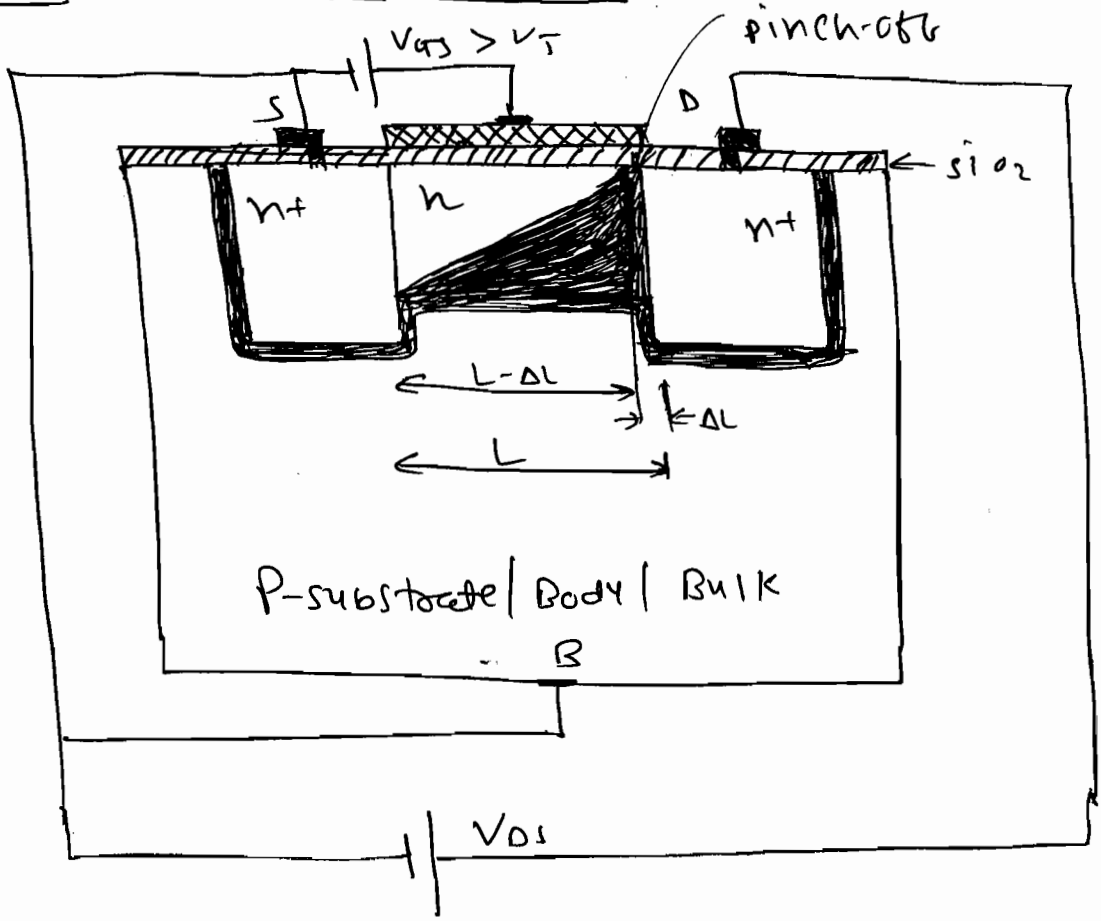




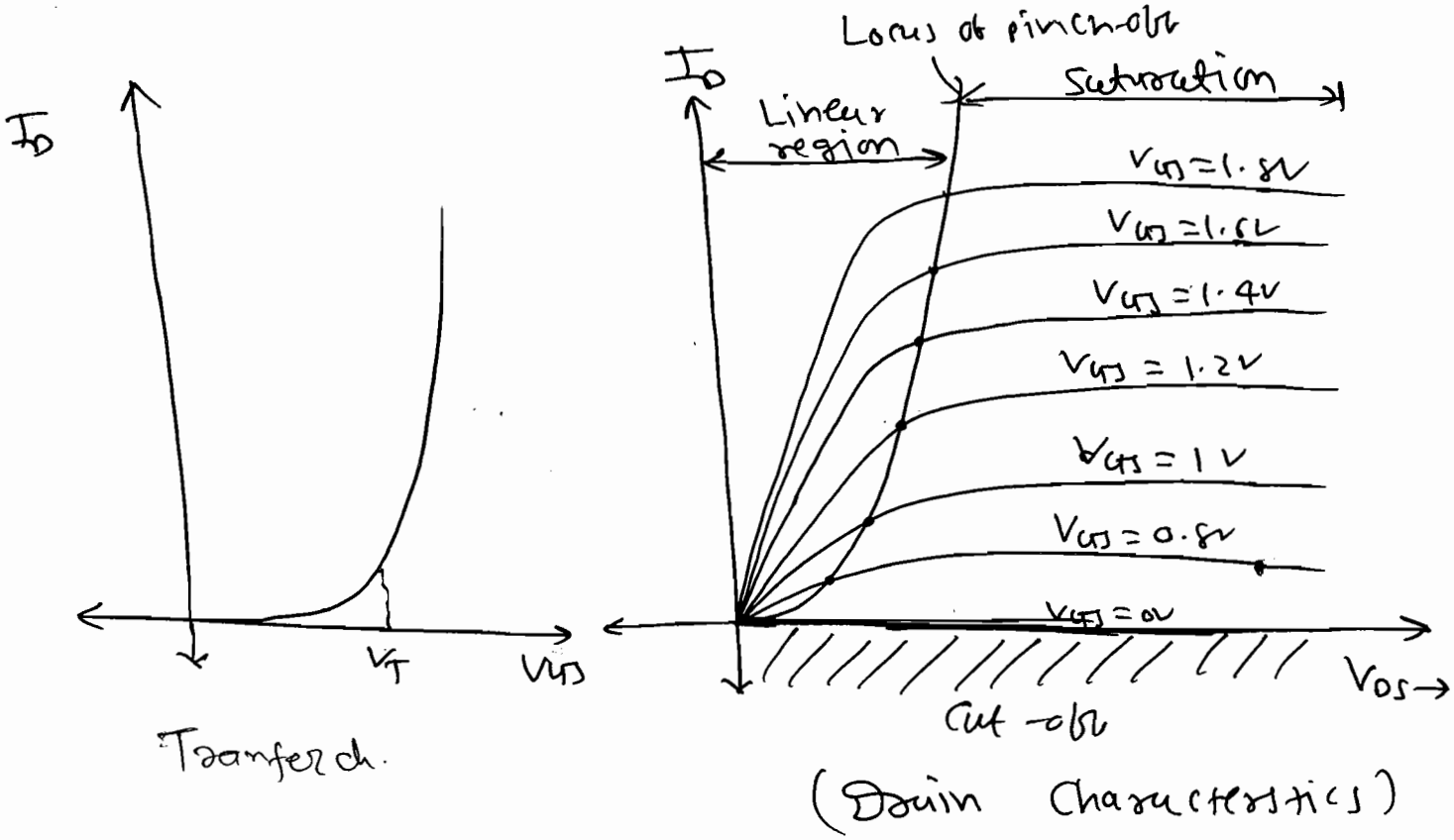
(ii) $V_{GS} > V_T$ & $V_{DS} < V_{GS} - V_T$. (Linear):



(iii) $V_{GS} > V_T$ & $V_{DS} > V_{GS} - V_T$. (Saturation):



* Drain and Transfer Characteristics:



⇒ From drain characteristics, only V_T & g_m can be extracted.

⇒ Channel Conductivity $\propto (V_{GS} - V_T)$.

⇒ Drain Current (I_D) $\propto (V_{GS} - V_T)$.

⇒ $\boxed{V_{DS} = V_{GS} - V_T}$

+ve +ve +ve.

$V_{DS} < V_{GS} - V_T$: Linear

$V_{DS} > V_{GS} - V_T$: Saturation.

⇒ <u>V_T, V_{GS} & V_{DS}:</u>

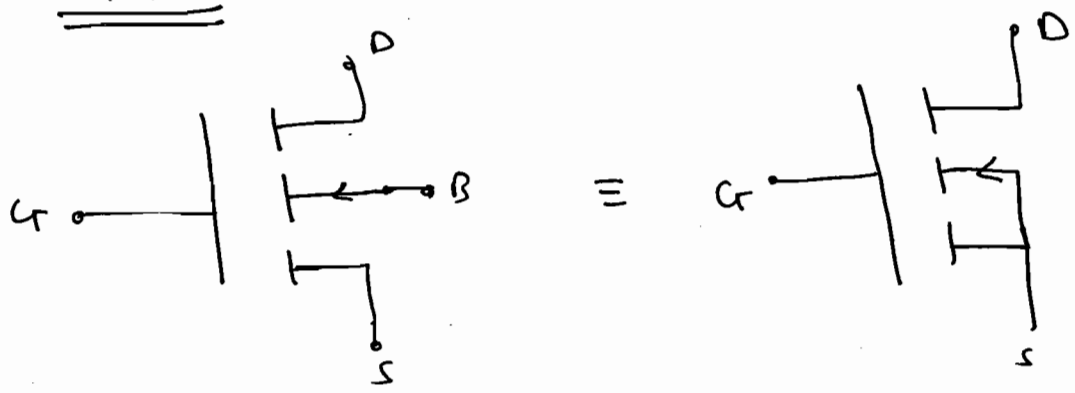
→ if $V_{GS} < V_T$: Cut-off.

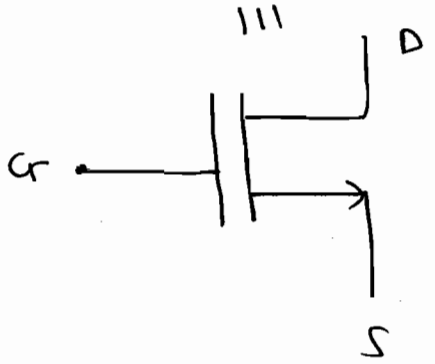
→ if $V_{GS} > V_T$

Calculate $V_{GS} - V_T$.

- if $V_{DS} < V_{GS} - V_T$: Linear
- if $V_{DS} \geq V_{GS} - V_T$: Saturation.

⇒ <u>Symbol:</u>





* Important points to be remember:

⇒ n- Channel E- MOSFET operates with +ve gate Voltages i.e. +ve V_{GS} value.

⇒ Gate to Source Voltage (V_{GS}) and Threshold Voltage (V_T) are +ve for n Channel enhancement MOSFET.

⇒ n- EMOSFET operate in enhancement mode for +ve V_{GS} values.

⇒ n- EMOSFET always operates in enhancement mode.

⇒ In descrete n- Channel EMOSFET, Substrate (or) Body is Connected to the ground or source terminal whereas in IC's it should be connected to the most -ve Voltage.

⇒ n- Channel EMOSFET will be on for +V_{GS} values (i.e. $V_{GS} > V_T$) and it will be off for 0 (or) -ve V_{GS} values. (i.e. $V_{GS} < V_T$).

⇒ At a given V_{GS} i.e. ($V_{GS} > V_T$) as drain to Source Voltage increases the width of the drain depletion region increases.

→ At a particular value of V_{DS}, the thickness of the channel near to drain becomes zero it is called pinch-off.

⇒ Condition for the pinch-off (or) sat is $V_{DS} = V_{GS} - V_T$. Here, all are +ve.

⇒ The Potential (or) Voltage across the Channel increases from source to drain end, therefore the R.B. b/w Channel and Substrate increases from source to drain end.

⇒ The width of the depletion region b/w Channel and substrate increases from source to drain end. Therefore the thickness of the channel decreases from source to drain end.

⇒ The inversion charge across the Channel decreases from source to drain end.

⇒ At pinch-off (or) Saturation the Channel is in tapered shape.

⇒ The electric field across the Channel remain constant at pinch off (or) at saturation.

⇒ Linear region also called by ohmic region (or) triode region.

⇒ Linear region is the region left side to the pinch-off Locus.

⇒ Saturation region is the region right side to the locus of pinch-off.

⇒ Cut-off region is the region below the $V_{GS} < V_T$.

⇒ MOSFET can be operate as an Amplifier in Saturation and it can be operate as a switch in Linear and Cut-off region.

⇒ MOSFET can be used as a Voltage Variable Resistor in linear region and it can be used as a current source in the saturation region.

⇒ Transfer Characteristics of a E-MOSFET gives V_T & g_m.

⇒ For $V_{GS} < V_T$, n-EMOSFET operates in Cut-off region and it drain current $I_D = 0A$.

⇒ For $V_{GS} > V_T$ & $V_{DS} < V_{GS} - V_T$ it operates in linear region and it drain current I_D is,

$$\Rightarrow \quad I_D = \mu_n C_{ox} \frac{W}{L}\left[(V_{GS}-V_T)V_{DS} - \frac{1}{2}V_{DS}^2\right].$$

(+ve, +ve, +ve)

→ C_{ox} : Oxide Capacitance per unit area.

C_{ox} : $\frac{\epsilon_{ox}}{t_{ox}}$.

t_{ox} : gate oxide thickness.

ϵ_{ox} : Permitivity of SiO_2.

ϵ_{rox} : $3.9 \approx 4$

ϵ_0 : 8.85×10^{-12} F/m.

ϵ_0 : 8.85×10^{-12} F/cm.

⇒ For $V_{GS} > V_T$ & $V_{DS} \geq (V_{GS}-V_T)$ it operates in Sat. region and its drain current.

$$I_D = \frac{1}{2}\mu_n . C_{ox} . \frac{W}{L}\left[(V_{GS}-V_T)\right]^2$$

(+ve, +ve)

Q - An n-channel enhancement MOSFET has $V_T = 0.7\,V$, and $V_{GS} = 1.5\,V$. Find the region of operation for $V_{DS} = 2.5$ volts.

Soln: Here, $V_T = 0.7\,V$, $V_{GS} = 1.5\,V$.

$V_{DS} = 2.5$

$\therefore V_{GS} > V_T$

and $V_{GS} - V_T = 1.5 - 0.7 = 0.8$.

$\therefore V_{DS} > (V_{GS} - V_T = 0.8)$

So, in Saturation.

Q - n-channel enhancement MOSFET has $V_T = 0.7\,V$ and $V_{GS} = 3V$. Find the region of operation for $V_{DS} = 2V$.

Soln: $V_{GS} = 3V$, $V_T = 0.7V$

$V_{GS} > V_T$

& $V_{GS} - V_T = 3 - 0.7 = 2.3V$

$(V_{DS} = 2V) < (V_{GS} - V_T = 2.3V)$

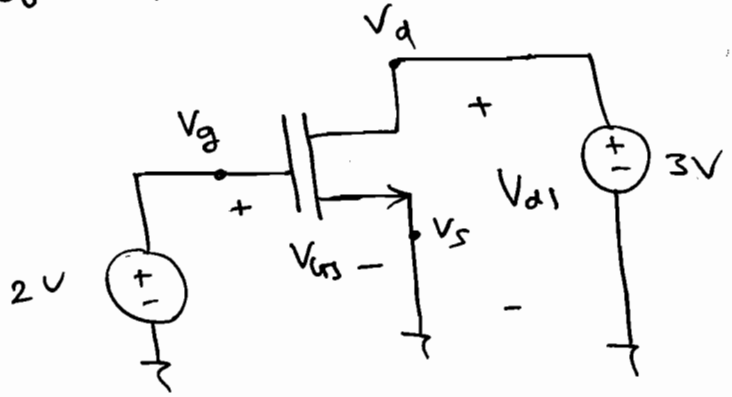
So, it operates in linear region.

Q: n-EMOSFET has $V_{GS} = 1.2V$ & $V_T = 1.5V$. Find region of operation for $V_{DS} = 4V$.

Soln: $V_{GS} = 1.2V$, $V_T = 1.5V$

$V_{GS} < V_T \Rightarrow$ it operates in cutoff region.

Q For the ckt shown in the figure. MOSFET has threshold voltage 0.6V. Find the region of operation.



Soln:

By KVL $2 - V_{GS} = 0$ & $V_{DS} - 3 = 0$

$\boxed{V_{GS} = 2V}$ $\boxed{V_{DS} = 3V}$

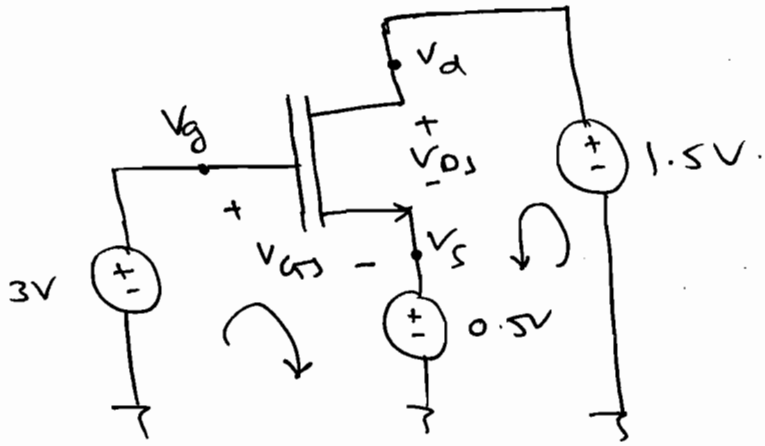
$V_T = 0.6V$

So, as $V_{GS} > V_T$ & $V_{GS} - V_T = 2 - 0.6 = 1.4$

$\therefore V_{DS} > (V_{GS} - V_T = 1.4)$

So, it operates in saturation.

Q For the ckt shown in the fig. MOSFET has $V_T = 0.6$. Find the region of operation.



Soln: By KVL, $3 - V_{GS} - 0.5 = 0 \Rightarrow \boxed{V_{GS} = 2.5V}$

By KVL, $1.5 - V_{DS} - 0.5 = 0$

$\Rightarrow \boxed{V_{DS} = 1V}$ & $V_T = 0.6$ (given).

Now. $V_{GS} = 2.5 > (V_T = 0.6V)$

$V_{GS} - V_T = 2.5 - 0.6 = 1.9V$

$\therefore (V_{DS} = 1) < (V_{GS} - V_T = 1.9)$

Therefore, it operates in linear region.

* Imp:

① Linear:

$$\Rightarrow I_D = \mu_n \cdot C_{ox} \cdot \frac{W}{L} \left[(V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right].$$

$$\Rightarrow \boxed{I_D = K_n' \cdot \frac{W}{L} \left[(V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right]}$$

where, $\boxed{K_n' = \mu_n \cdot C_{ox}}$ (A/V^2).

$$K_n' = \frac{I_D}{(V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2} \cdot \quad (A/V^2).$$

$$\Rightarrow \boxed{I_D = \beta_n \left[(V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right]}$$

$\beta_n = \mu_n \cdot C_{ox} \cdot \frac{W}{L}$ A/V^2

$\boxed{\beta_n = K_n' \cdot \frac{W}{L}}$ A/V^2.

$\Rightarrow K_n' = K'$, $\beta_n = \beta = K$.

② Saturation:

$$\Rightarrow I_D = \frac{1}{2} \mu_n \cdot C_{ox} \cdot \frac{W}{L} \left[V_{GS} - V_T \right]^2.$$

$$\boxed{I_D = \frac{1}{2} \cdot K_n' \cdot \frac{W}{L} \left[V_{GS} - V_T \right]^2.}$$

$$\Rightarrow \boxed{I_D = K_n \left[V_{GS} - V_T \right]^2.}$$

$$K_n = \frac{1}{2}\mu_n . C_{ox} . \frac{W}{L} . (A/V^2).$$

$$K_n = \frac{1}{2} K_n' . \frac{W}{L} . (A/V^2).$$

$$I_D = \frac{1}{2}\beta_n [V_{GS} - V_T]^2 \quad , \quad \beta_n = \mu_n C_{ox} . \frac{W}{L} \ (V/m^2)$$

* Deep Triode Region:

=> Deep triode region is also a linear region but for small values of V_{DS}.

=> Condition for Deep Triode Region is,

$$\therefore \boxed{V_{DS} << 2[V_{GS} - V_T].}$$

$$\Rightarrow I_D = \mu_n C_{ox} . \frac{W}{L} . \left[[V_{GS} - V_T] V_{DS} - \frac{1}{2} V_{DS}^2 \right].$$

in linear region.

for deep triode region it is given by.

$$\therefore I_D = \mu_n C_{ox} . \frac{W}{L} \times [(V_{GS} - V_T) V_{DS}].$$

$$\boxed{I_D = K_n' . \frac{W}{L} \times (V_{GS} - V_T) . V_{DS}.}$$

$$I_D = \beta_n (V_{GS} - V_T) V_{DS}.$$

$$K_n' = \mu_n . C_{ox}.$$

$$\beta_n = \mu_n . C_{ox} \times \frac{W}{L} = K_n' . \frac{W}{L}.$$

$$K_n = K = \beta_n = K_n' . W/L = \mu_n . C_{ox} . \frac{W}{L}.$$

* Drain ON Resistance (or) ON resistance (or) Drain to Source resistance.

⇒ $r_{ds(ON)}$, (or) $r_{d(ON)}$, (or) $R_{(ON)}$.

⇒ Pinch-off point in drain characteristic of MOSFET is also called V_{DS} (or) V_{DSmin} (or) V_{DSat} (or) over drive Voltage

$$V_{ov} = V_{GS} - V_T$$

⇒ It is the resistance offered by the MOSFET in the Linear region for small values of V_{DS}.

⇒ It is the reciprocal of the slope of the drain characteristic in the linear region for small value of V_{DS}.

$$r_{ds(ON)} = r_{d(ON)} = R_{ON} = \frac{1}{\frac{\Delta I_D}{\Delta V_{DS}}}$$

$$\therefore \boxed{R_{ON} = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS}}}$$

$$\boxed{R_{ON} = \left.\frac{dV_{ds}}{dI_D}\right|_{V_{GS}}}$$

⇒ $I_D = \mu_n . C_{ox} . \frac{W}{L} [V_{GS} - V_T] V_{DS}$.

$$\therefore \frac{dI_D}{dV_{DS}} = \mu_n . C_{ox} . \frac{W}{L} (V_{GS} - V_T).$$

$$\therefore R_{ON} = r_{d(ON)} = r_{ds(ON)} = \frac{1}{\mu_n C_{ox} \cdot \frac{W}{L} (V_{GS} - V_T)}$$

$$= \frac{1}{K_n' \cdot \frac{W}{L} (V_{GS} - V_T)}$$

$$= \frac{1}{\beta_n \cdot (V_{GS} - V_T)}$$

$(V_{GS} - V_T) = V_{OV}$ ← overdrive voltage

$$\therefore \boxed{R_{ON} \propto \frac{1}{(W/L)}}$$

$$\boxed{C \propto \frac{W}{L}}$$

* Trans Conductance (g_m):

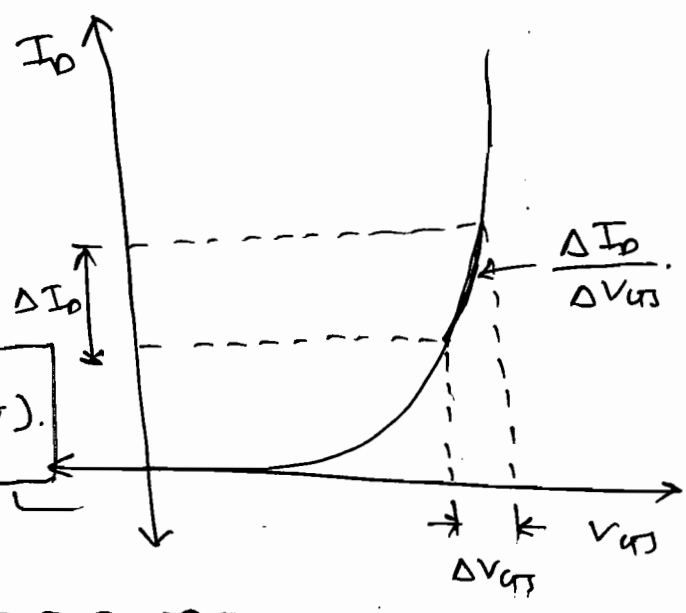
⇒ Trans Conductance is also called as mutual Conductance (or) Figure of merit.

⇒ It gives how effectively MOSFET converts the voltage changes at input to the corresponding current changes at the output in saturation region.

⇒ Trans Conductance is also equal to the slope of the transfer characteristics.

⇒ $I_D = \frac{1}{2} \mu_n C_{ox} \cdot \frac{W}{L} [V_{GS} - V_T]^2$.

$$\therefore \frac{dI_D}{dV_{GS}} = \mu_n C_{ox} \cdot \frac{W}{L} [V_{GS} - V_T].$$



$$\therefore \boxed{g_m = \frac{dI_d}{dV_{GS}} = \mu_n C_{ox} \cdot \frac{W}{L} (V_{GS} - V_T).} \quad -①$$

$$\therefore \boxed{g_m = \frac{1}{R_{ON}}}$$

$$\Rightarrow \boxed{g_m = \sqrt{2\mu_n \cdot C_{ox} \cdot \frac{W}{L} \cdot I_D} \quad - (2).} \quad - (2)$$

g_{m2} $2k_n(V_{GS}-V_T)$

$$\Rightarrow g_m = \sqrt{2\mu_n \cdot C_{ox} \cdot \frac{W}{L}} \cdot \sqrt{\frac{1}{2}\mu_n C_{ox} \times \frac{W}{L} \cdot (V_{GS}-V_T)^2}.$$

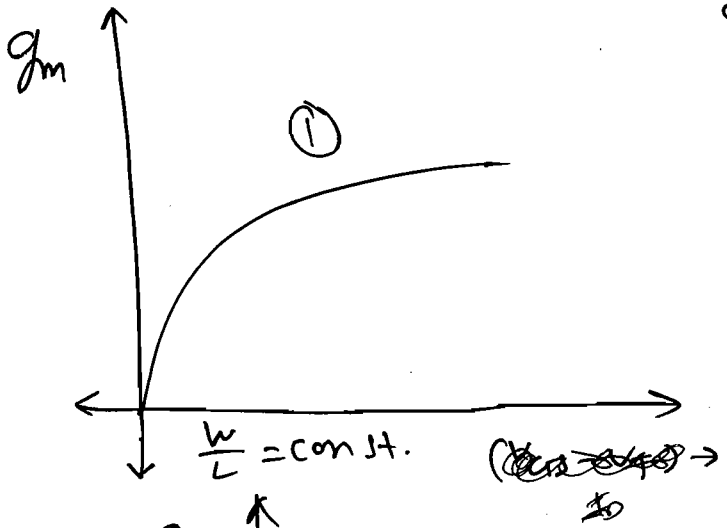
$$\therefore g_m = \sqrt{2\mu_n \cdot C_{ox} \cdot \frac{W}{L} \cdot I_D} \quad (A|V)$$

$$\Rightarrow \boxed{g_m = \frac{2I_D}{V_{GS}-V_T}} \quad - (3).$$

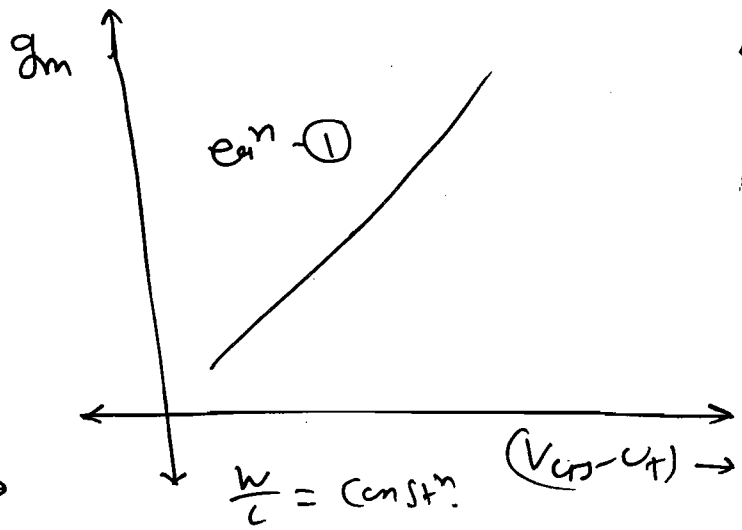
$$\rightarrow g_m = \frac{2 \cdot \frac{1}{2} \cdot \mu_n \cdot C_{ox} \cdot \frac{W}{L} (V_{GS}-V_T)^2}{(V_{GS}-V_T)}$$

$$\therefore \boxed{g_m = \frac{2I_D}{V_{GS}-V_T}}$$

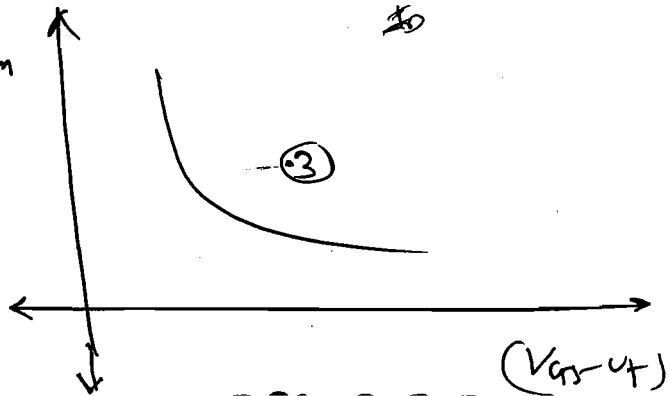
⊛ eqn-(1)



⊛ eqn-(2)

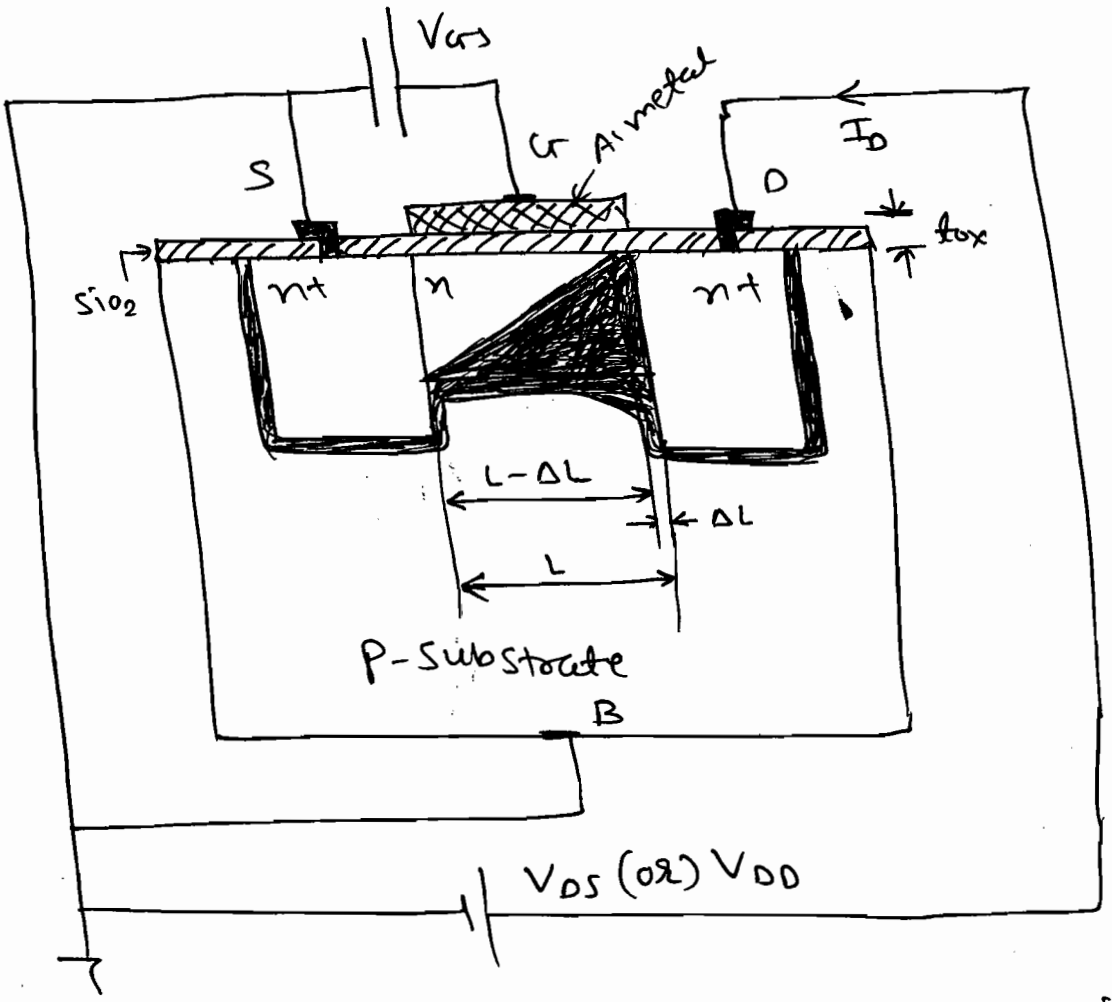


* eqn-(3)



* Channel Length Modulation:

⇒



⇒ In the saturation region as drain to source increases the effective length of the channel decreases i.e. as V_{DS} varies the length of the channel is varies it is called channel length modulation.

⇒ Due to channel length modulation Drain current increases and it is given by

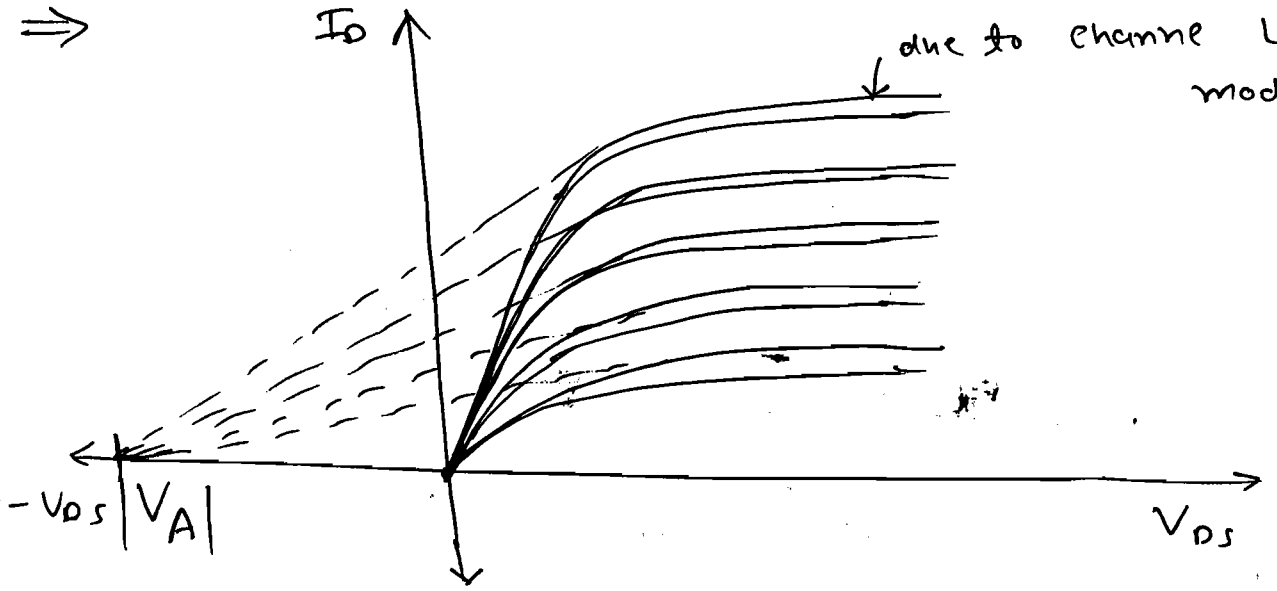
$$I_D = \frac{1}{2} \mu_n \cdot C_{ox} \cdot \frac{W}{L} [V_{GS} - V_T]^2 (1 + \lambda V_{DS}).$$

$\lambda = \frac{1}{V_A}$; V_A = early Voltage.

$V_{GD} = V_{GS} - V_{DS} > V_T$

Required $\rightarrow V_{GD} = V_{GS} - V_{DS} = V_T$

⇒



* Drain Resistance (or) o/p resistence :

r_d (or) R_o:

⇒ It is the resistance offered by the MOSFET in the saturation region.

⇒ It is the reciprocal of the slope of drain characteristics in the saturation region.

⇒ Slope $= \left.\frac{\Delta I_D}{\Delta V_{DS}}\right|_{V_{GS}}$

$$r_d \text{ (or) } r_o = \left.\frac{1}{\frac{\Delta I_D}{\Delta V_{DS}}}\right|_{V_{GS}} = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS}} = \left.\frac{dV_{DS}}{dI_D}\right|_{V_{GS}}.$$

$$r_d \text{ (or) } r_o = \frac{1}{\lambda I_D}$$

$$\Rightarrow I_D = \frac{1}{2}\mu_n \cdot C_{ox} \cdot \frac{W}{L}\left[(V_{GS}-V_T)^2\right](1+\lambda V_{DS}).$$

$$\therefore \frac{dI_D}{dV_{DS}} = \underbrace{\frac{1}{2}\mu_n \cdot C_{ox} \cdot \frac{W}{L}\left[V_{GS}-V_T\right]^2}_{I_D \text{ (without channel length modulation)}} \cdot \lambda.$$

$$\therefore \frac{dI_D}{dV_{DS}} = \lambda . I_D .$$

$$\therefore \boxed{r_d \text{ (or) } r_o = \frac{1}{\lambda I_D} = \frac{V_A}{I_D} \quad (\because \lambda = \frac{1}{V_A}).}$$

⇒ Drain resistance (or) O/P resistance is also called A.C. resistance (or) small signal resistance.

* Body effect:

→ due to Body effect $V_T \uparrow$

⇒ V_{SB} : Source to Body Voltage.

V_{TO} : Threshold Voltage of MOSFET when $V_{SB} = 0$.

$$\boxed{V_T = V_{TO} + \gamma \left[\sqrt{V_{SB} + \phi_s} - \sqrt{\phi_s} \right].}$$

V_T : Threshold voltage of MOSFET of a given V_{SB}.

ϕ_s : Surface potential, $\phi_s = 2 v_T \ln \left(\frac{N_A}{n_i} \right)$.

v_T : Thermal voltage.

v_T : $\frac{T}{11,600} = \frac{300}{11,600} = 0.02586 \approx$ 26mV.

$\boxed{\gamma : \text{Body effect Co-efficient.}}$

$$\boxed{\gamma = \frac{\sqrt{2 q N_A \cdot \epsilon_{si}}}{C_{ox}}}, \quad C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}.$$

$$\therefore \boxed{\gamma = \frac{t_{ox}}{\epsilon_{ox}} \cdot \sqrt{2 q N_A \epsilon_{si}}}$$

$t_{ox} \uparrow \rightarrow V_T \uparrow$	$V_{SB} \uparrow \longrightarrow V_{SB} \uparrow$	(NA or ND) $\uparrow \rightarrow V_T \uparrow$
$t_{ox} \downarrow \rightarrow V_T \downarrow$	$V_{SB} \downarrow \longrightarrow V_{SB} \downarrow$	(NA or ND) $\downarrow \rightarrow V_T \downarrow$

⇒ Due to body effect threshold voltage increases. Therefore drain current decreases.

* Temperature effect:

⇒ V_T & $K_n' = \mu_n C_{ox}$.

⇒ Case-(i): V_T

V_T : dependent on Temperature.

V_T : dec by 2mV/°C.

$T \uparrow \longrightarrow V_T \downarrow \longrightarrow I_D \uparrow$

PTC

$T \uparrow \rightarrow I_D \downarrow$

NTC

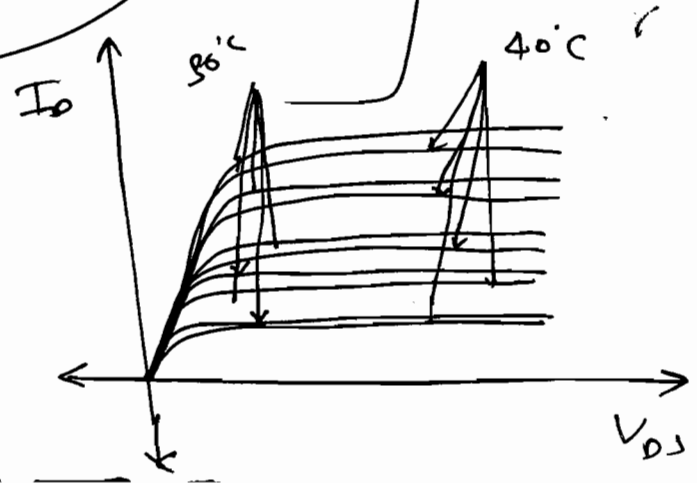
⇒ Case-(ii):

$\rightarrow K_n' = \mu_n C_{ox}$.

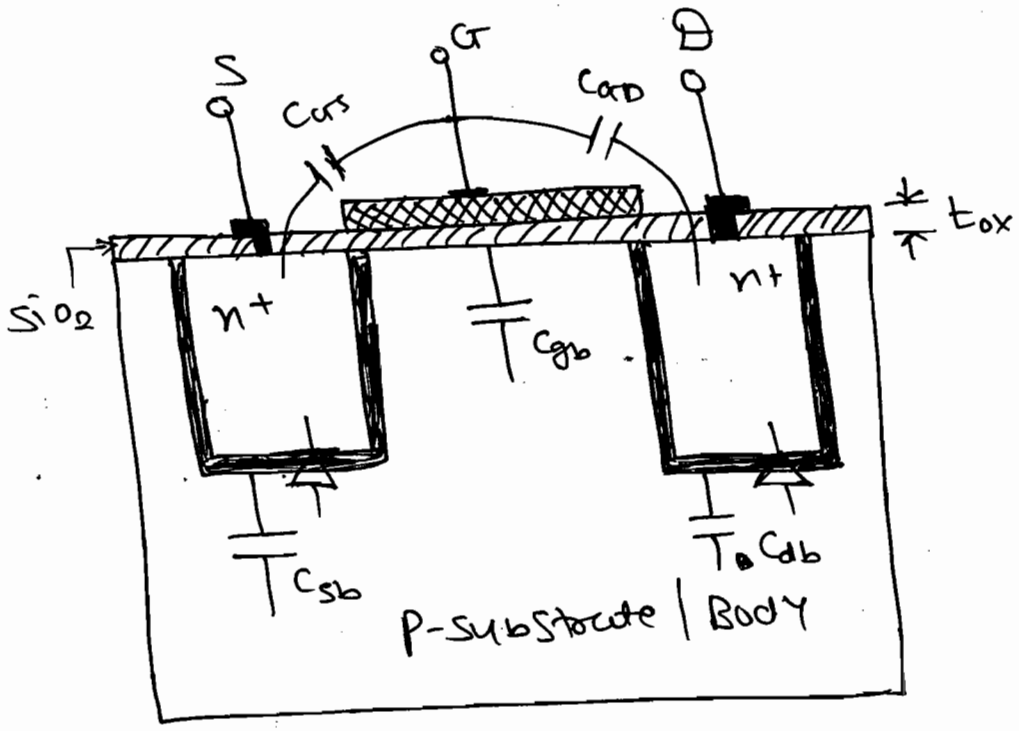
$\mu_n \propto \frac{1}{T^m} \Rightarrow \mu \propto T^{-m}$.

$T \uparrow \longrightarrow \mu_n \downarrow \longrightarrow I_D \downarrow$

NTC



* Mos Capacitor: Imp:



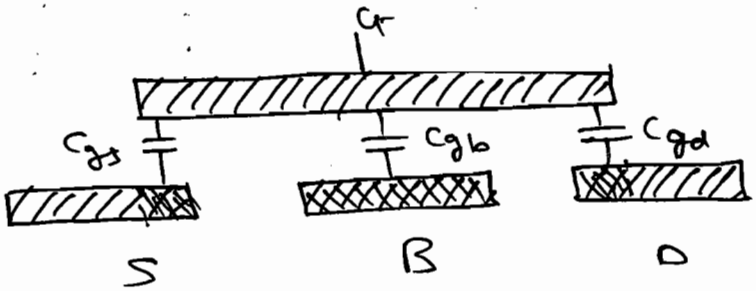
① Gate Capacitors:

(i) Gate to Source Cap. (C_{gs})

(ii) Gate to drain Cap. (C_{gd}).

(iii) Gate to body Cap. (C_{gb}).

⇒



$C_g = C_{gs} + C_{gd} + C_{gb}$.

C_g: Total gate capacitance.

② junction Capacitors:

(i) Source to body junction Cap. (C_{sb}).

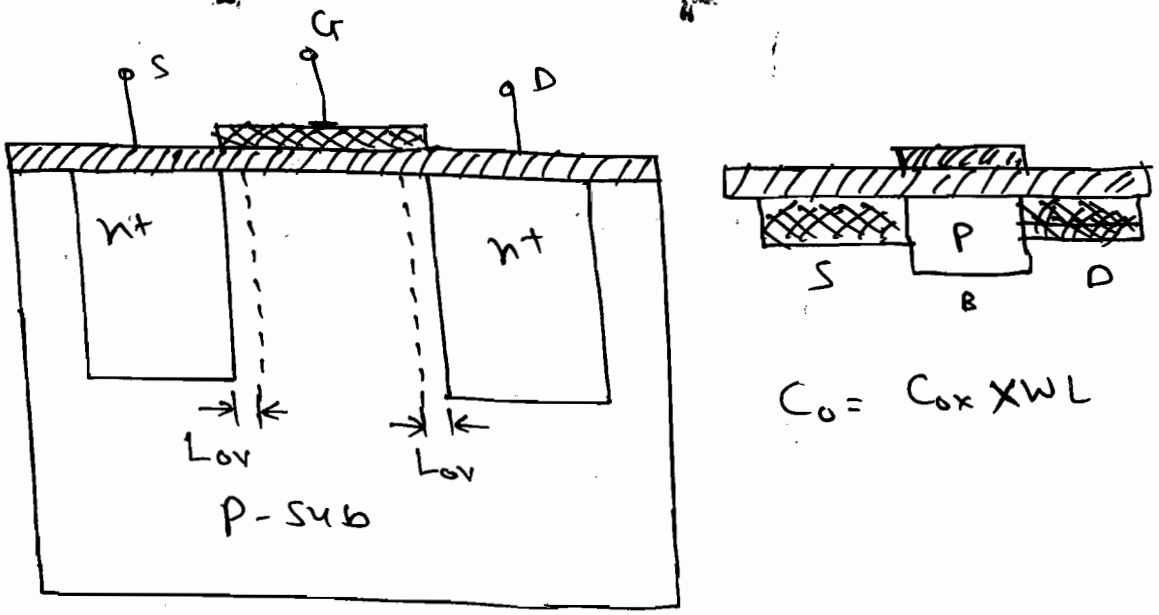
(ii) Drain to Body junction Cap. (C_{db}).

1. Gate Capacitors:

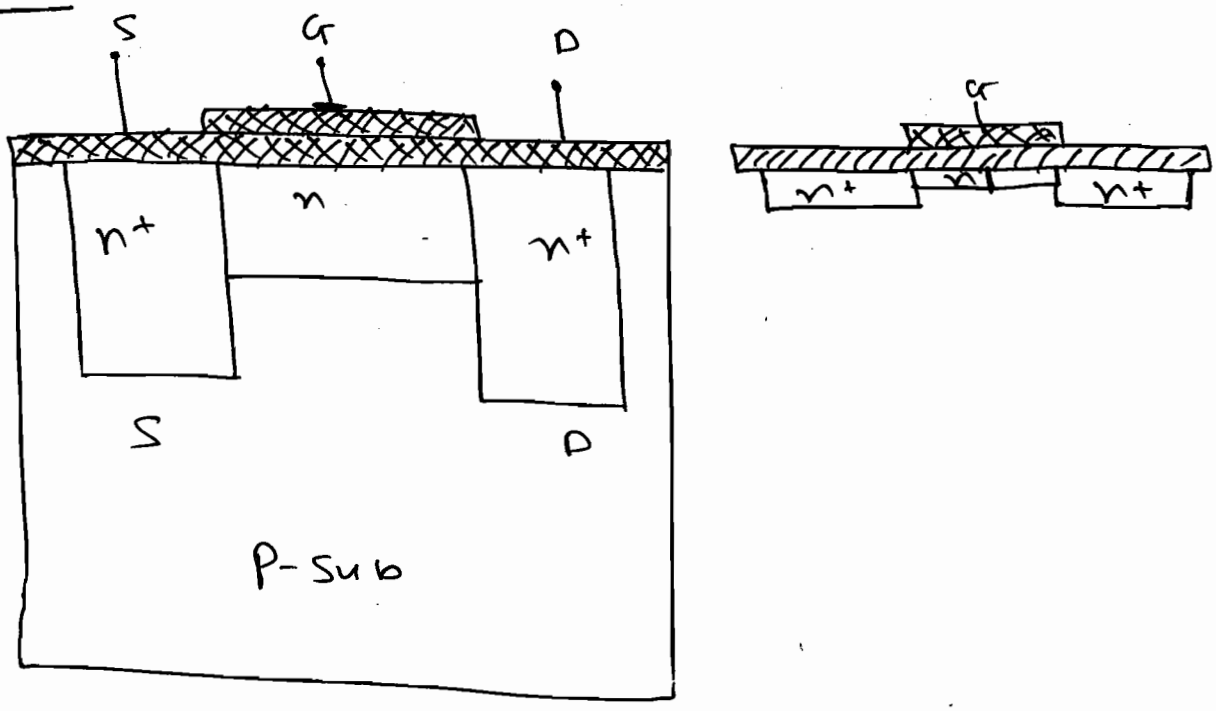
→ $C_{gs} = 0 + C_{ox}.WL_{ov}$ * Cut-off:

$C_{gd} = 0 + C_{ox}.WL_{ov}$

$C_{gb} = C_{ox}.WL$



* Linear:



$C_{gs} = \frac{1}{2} C_{ox}.WL + C_{ox}WL_{ov}$

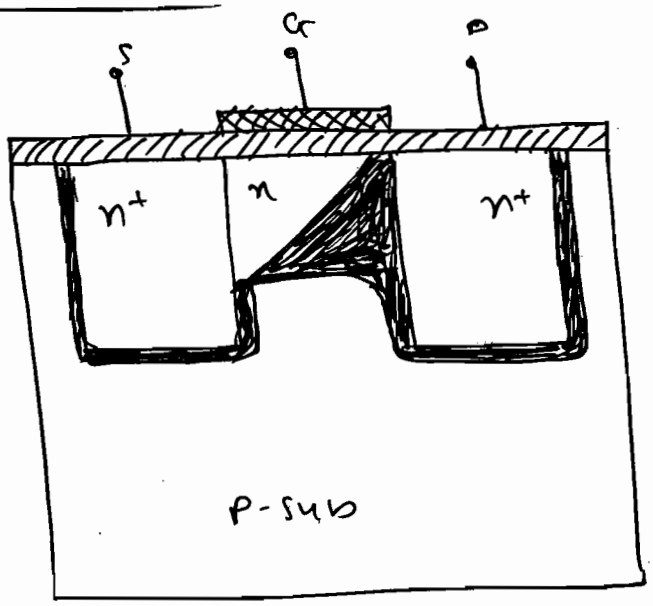
$C_{gd} = \frac{1}{2} C_{ox}WL + C_{ox}.WL_{ov}$

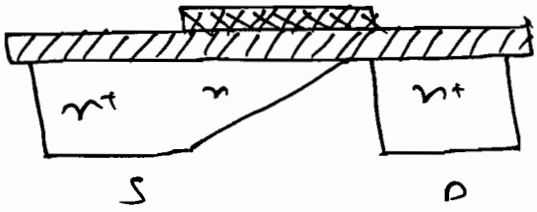
$C_{gb} = 0$

$L_{eff} = L - 2\Delta L_{ov}$.

Here, L is bydefaut eff. length

* Saturation:





$$\Rightarrow C_{gs} = \frac{2}{3} C_{ox} WL + C_{ox} \cdot WL_{ov}.$$

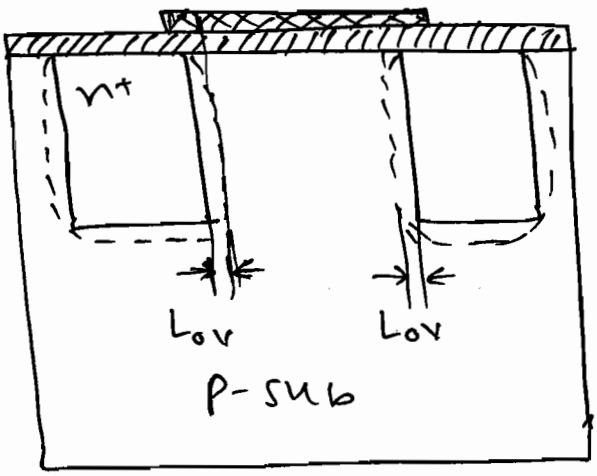
$$C_{gd} = C_{ox} \cdot WL_{ov}.$$

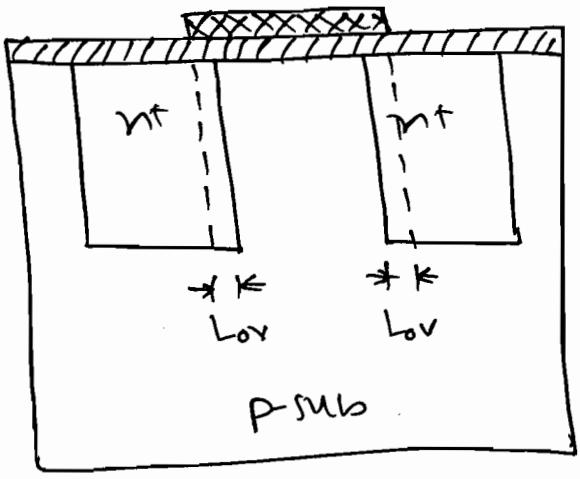
$$C_{gb} = 0.$$

$\Rightarrow$

Cap	Cut off	Linear	Saturation
C_{gs}	0	$\frac{1}{2} C_o$	$\frac{2}{3} C_o$
C_{gd}	0	$\frac{1}{2} C_o$	0
C_{gb}	C_o	0	0
C_g	C_o	C_o	$\frac{2}{3} C_o$

* L_{ov}: overlape Length:

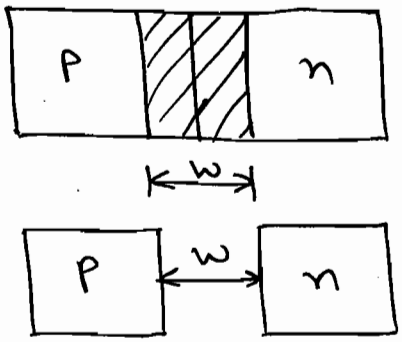




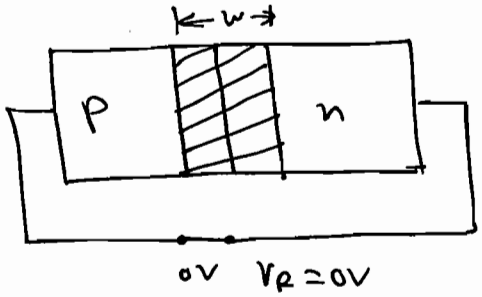
$$C_{ov} = C_{ox} W L_{ov}$$

2. Junction Capacitors:

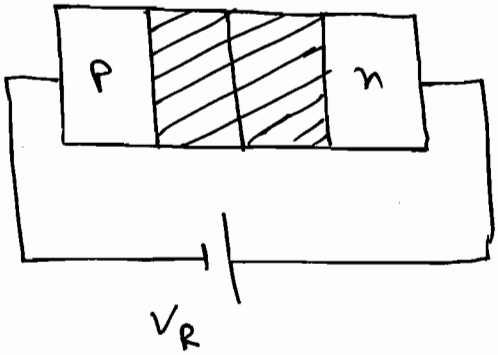
⇒ It is also called as Depletion Capacitance (or) Space Charge Capacitance.

① 

$$C_T = \frac{\epsilon A}{W}$$

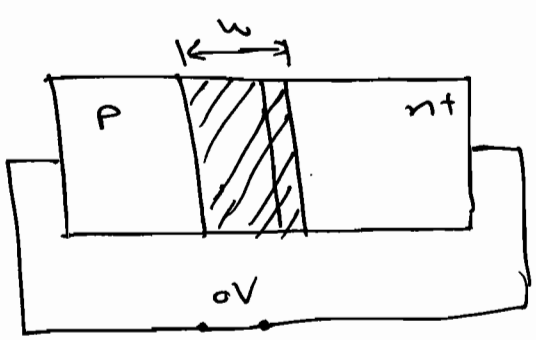
② 

$$C_{T0} = \frac{\epsilon A}{W}$$

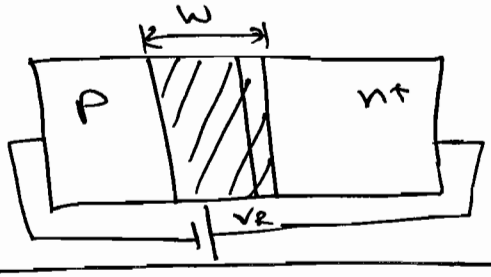
③ 

$$C_T = \frac{C_{T0}}{\left[1 + \frac{V_R}{V_0}\right]^{1/3}}$$

$$C_{j0} = \frac{c_{j0}}{\left[1 + V_R/V_0\right]^{1/3}}$$

① 

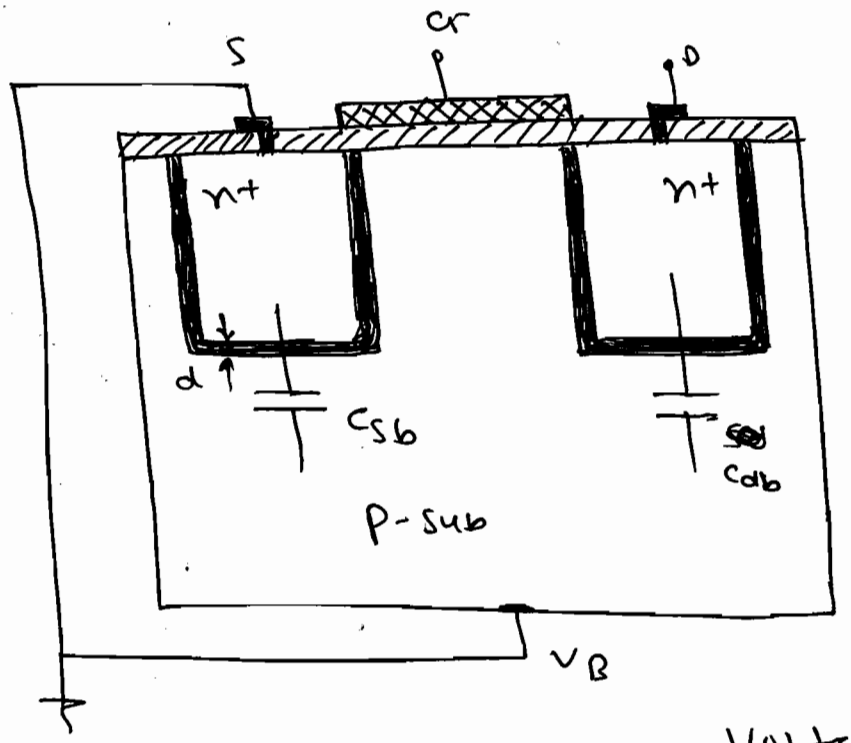
$$C_{T0} = \frac{\epsilon A}{W} \; ; \; C_{j0} = \frac{\epsilon A}{W}$$

② 

$$C_j = \frac{C_{T0}}{\left[1 + \frac{V_R}{V_0}\right]^{1/2}}$$

$$C_j = \frac{c_{j0}}{\left[1 + \frac{V_R}{V_0}\right]^{1/2}}$$

(i) Source to Body junction Capacitance:-



⇒ V_{SB}: Source to body Voltage.

$$C_{sbo} = \frac{\epsilon_{si} A}{d}.$$

C_{sbo}: Source to Body junction when $V_{SB} = 0V$

A: Common area b/w Source and Body.

d: depletion layer thickness b/w Source and Body.

ϵ_{si}: permitivity of Si

$\epsilon_{si} = \epsilon_{rsi} \cdot \epsilon_0$, $\epsilon_{rsi} = 11.7 \approx 12$.

$\epsilon_0 = 8.85 \times 10^{-12}$ F/m.

⇒
$$C_{sb} = \frac{C_{sbo}}{\left[1 + \frac{V_R}{V_0}\right]^{1/2}}.$$

∴
$$\boxed{C_{sb} = \frac{C_{sbo}}{\sqrt{1 + \frac{V_R}{V_0}}}}.$$

C_{sb}: Source to body Capacitance at a given V_{SB}.

V_o: Built in potential (or) contact potential.

Q Gate-2012:

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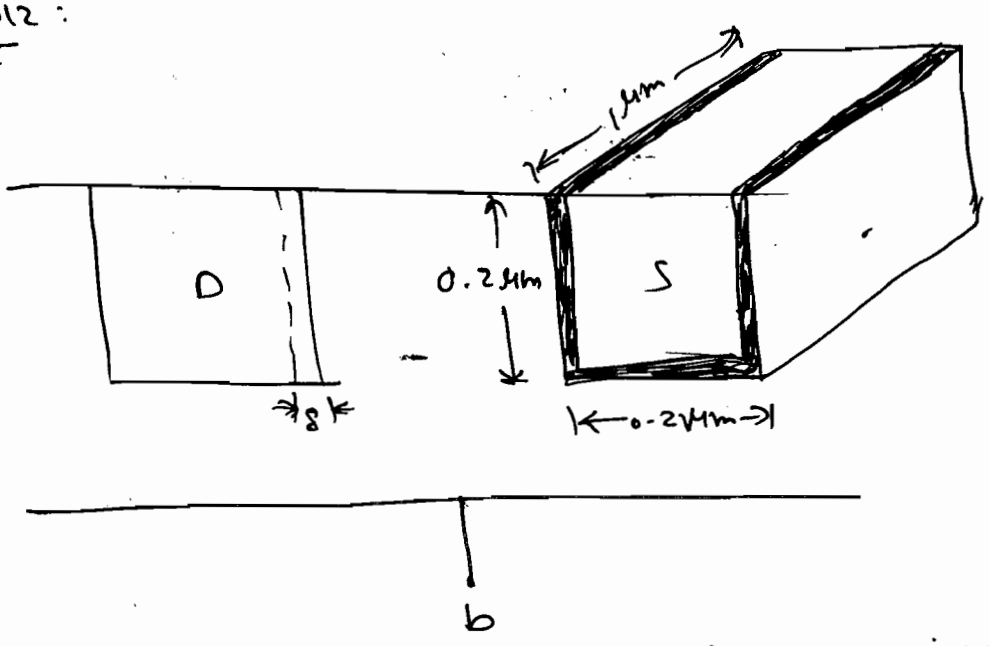


Obj

⇒ In 3-dimention there are three sides at which p-n jn is created. (i) bottom (ii) Left (iii) Right. So, we should consider Total area bet^n body and source for C_{sb} calculation.

∴ and here no biasing is provided

So, $C_{sb} = C_{sbo} = \frac{\epsilon_{si} \cdot A}{d}$.

$\therefore A = (0.2\mu \times 0.2\mu) + (0.2 \times 1\mu) + (0.2\mu \times 0\mu)$

$= 3 \times 0.2 \times 10^{-6} \times 1 \times 10^{-6}$

$\therefore A = 0.6 \times 10^{-12}\ m^2$.

$\therefore C_{sb} = \frac{11.7 \times 8.9 \times 10^{-12} \times 0.6 \times 10^{-12}}{10 \times 10^{-9}}$

$\therefore C_{sb} = 6.24 \times 10^{-15}$

$\therefore \quad C_{sb} = 6.24\ fF \approx 7\ fF$

if we consider front and back area then

$A = (3 \times 0.2 \times 10^{-12}) + (2 \times 0.2 \times 0.2 \times 10^{-12})$

$A = 0.68 \times 10^{-12}\ m^2$

&

$\boxed{C_{sb} = 7.024\ fF}$

Q-9

Soln:

$$C_{gs_{ov}} = \frac{\epsilon_{sio_2} W L_{ov}}{d}$$

$$C_{gs_{ov}} = \frac{3.9 \times 8.9 \times 10^{-12} \times 10^{-6} \times 20 \times 10^{-9}}{10 \times 10^{-9}}$$

$\therefore \boxed{C_{gs_{ov}} = 0.7\ fF.}$

2. Drain to Body jn Capacitor:

$\Rightarrow V_{dB}$ = Drain to Body voltage.

$$C_{db_0} = \frac{\epsilon_{si} A}{d}$$

C_{DB0} = drain to body capacitance when $V_{SB} = 0$.

d : depletion layer thickness bet^n D & S.

A : Common area bet^n D & S.

ϵ_{si} : permitivity of Si

$\epsilon_{si} = \epsilon_{rsi} \cdot \epsilon_0$, $\epsilon_{rsi} = 11.7 \simeq 12.$

$\epsilon_0 = 8.85 \times 10^{-12}$ F/m.

$\Rightarrow$ $$C_{db} = \frac{C_{db0}}{\sqrt{1 + \frac{V_{db}}{V_0}}}$$

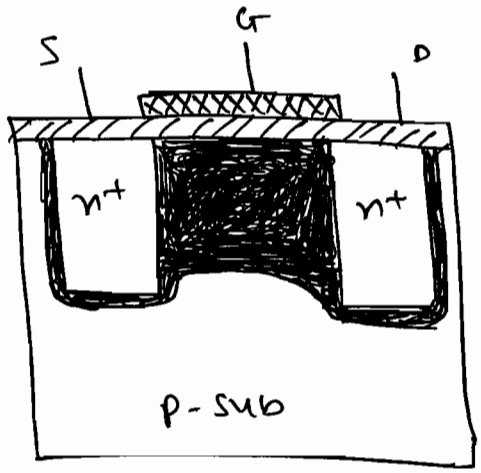
C_{dB} : Drain to body capacitor with at a given V_{dB}.

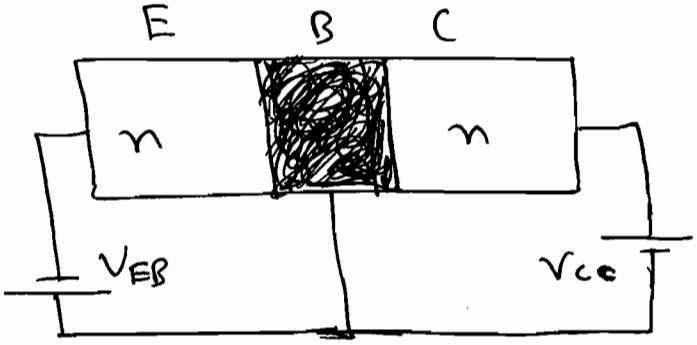
V_0 : Built in potential at constant potential.

* Short Channel effect :-

1. Punch through:

$\Rightarrow$

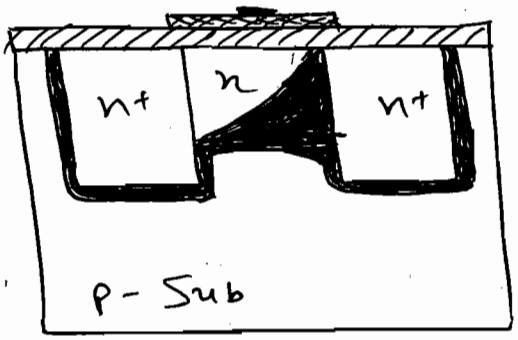




$\Rightarrow$ For short channel MOSFET in the saturation region as drain to source voltage increases. The width of the drain depletion region increases. At a particular value of V_{DS}, drain depletion region penetrates through channel to the source. It is called punch through (or) Reach-through.

2. Avalanch Break Down:

⇒



⇒ As drain to source voltage increases, the width of the drain depletion region increases. At a particular value of V_{DS} this depletion region gets breakdown due to avalanch effect. Therefore, it is called avalanch effect.

⇒ Due to punch through effect (or) avalanch Breakdown, the MOSFET never gets damage.

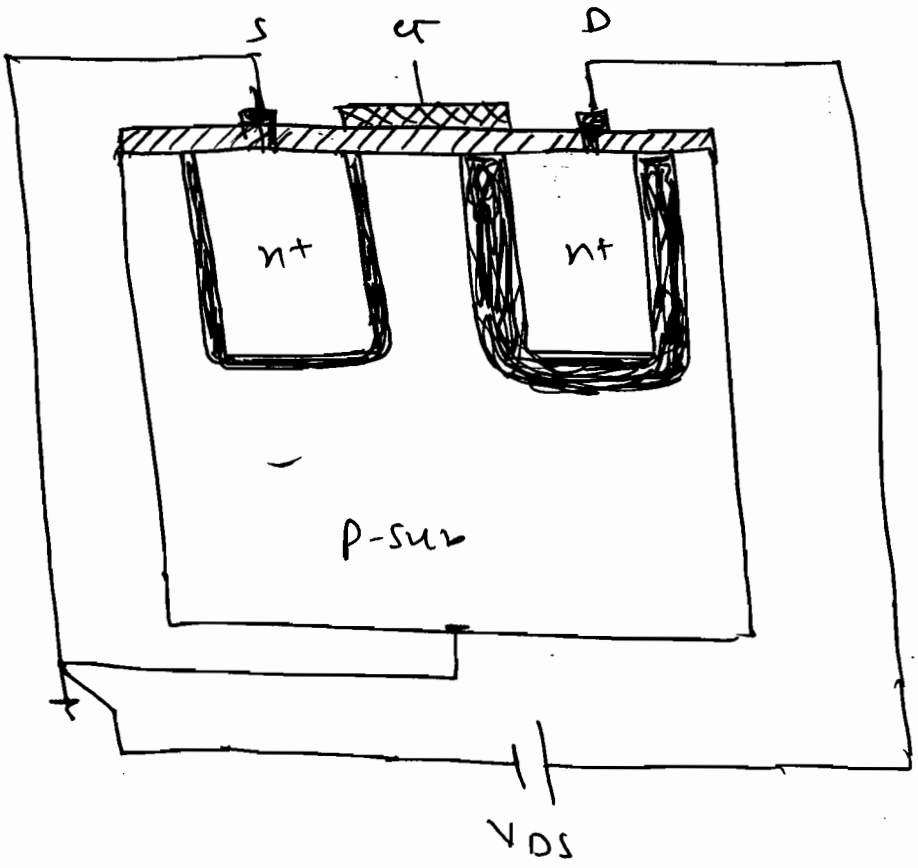
3. Gate - oxide Break- Down:

⇒ As gate to source voltage increases at a particular value of V_{GS} the oxide layer bet^n gate and source gets damage (or) Breakdown it is called gate - oxide Breakdown.

⇒ Gate oxide B-D is a permenant damage to the MOSFET.

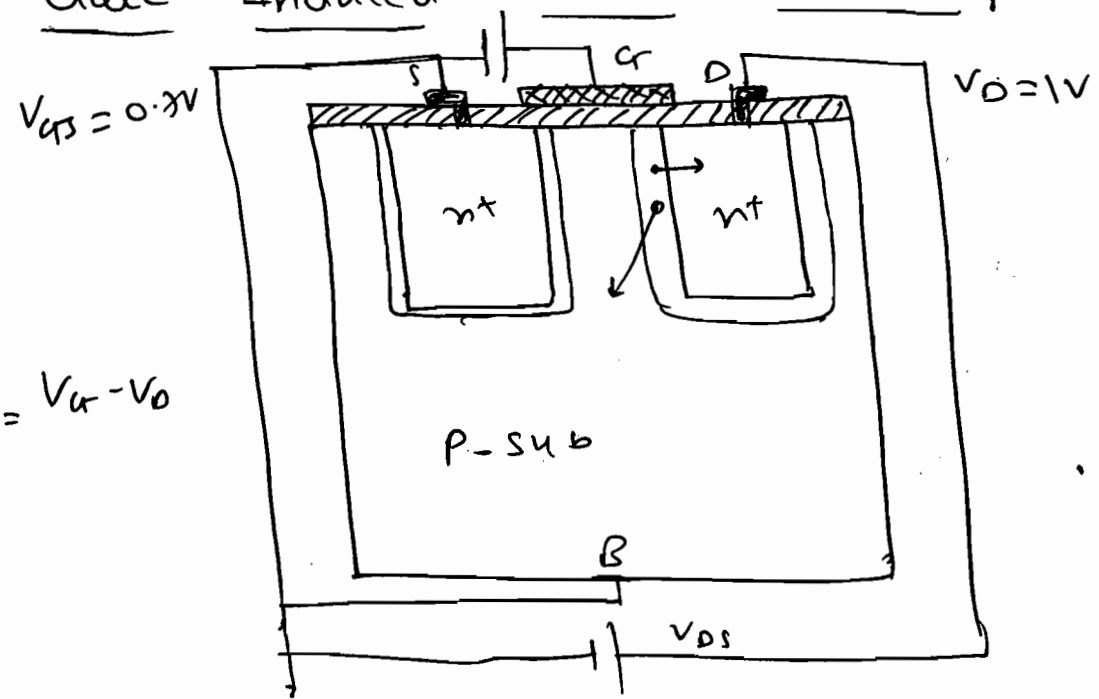
4. Drain Induced Barrier Lowering (DIBL):

⇒



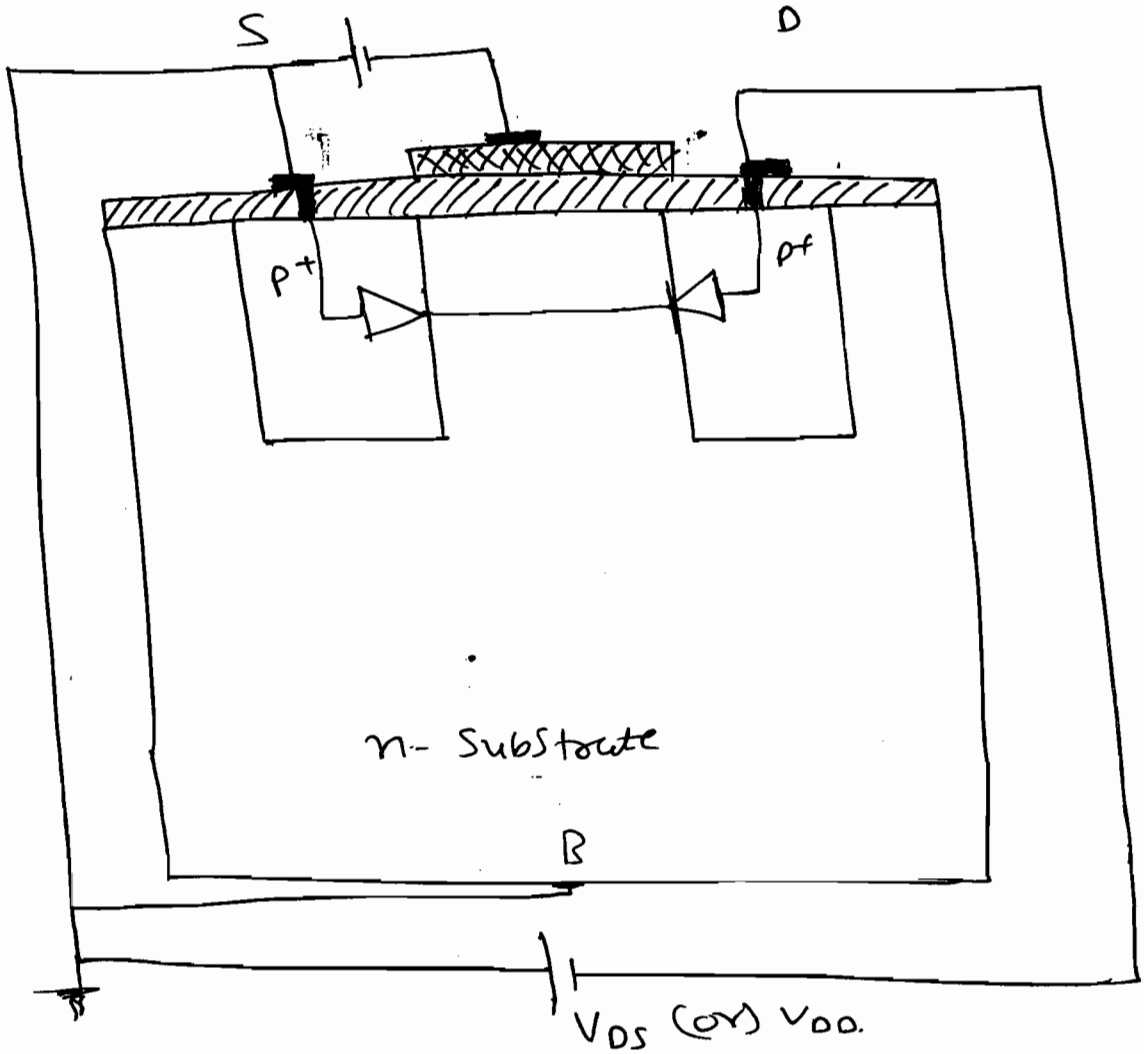
⇒ As drain to source voltage increases, the width of the drain depletion region increases. Therefore, threshold voltage decreases. i.e. it forms a channel for lower value of V_{GS}.

5. Gate Induced drain Leakage: (GIDL).

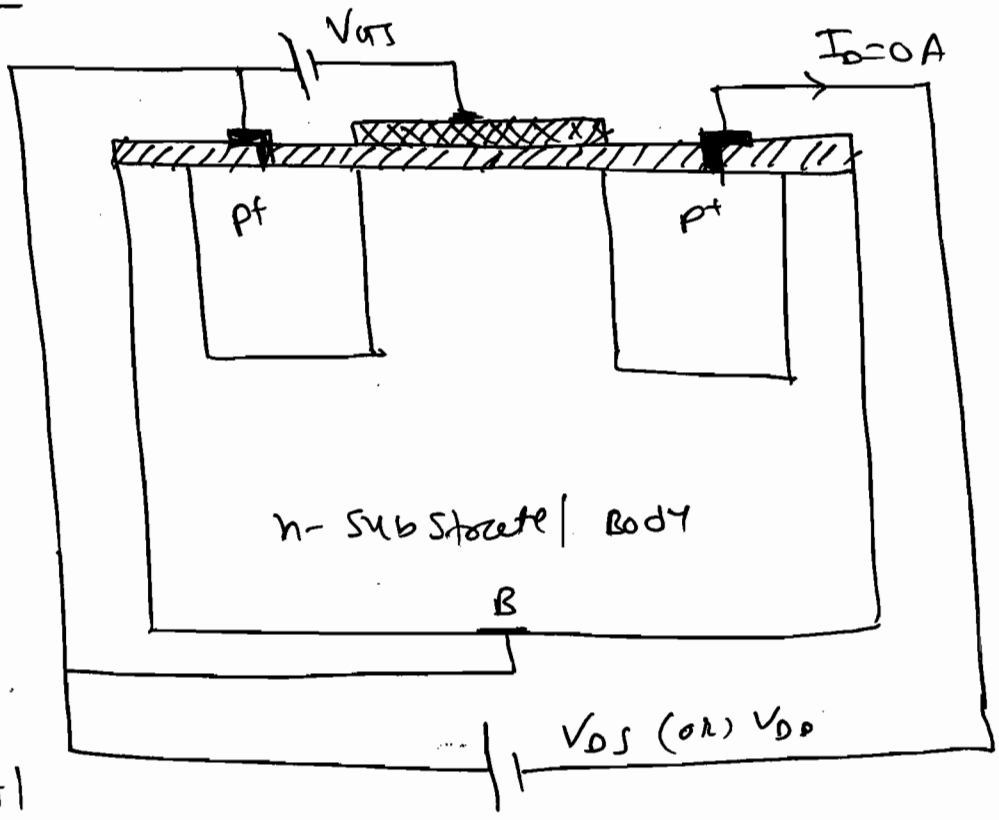


$V_{GD} = V_G - V_D$

* P- channel Enhancement MOSFET:

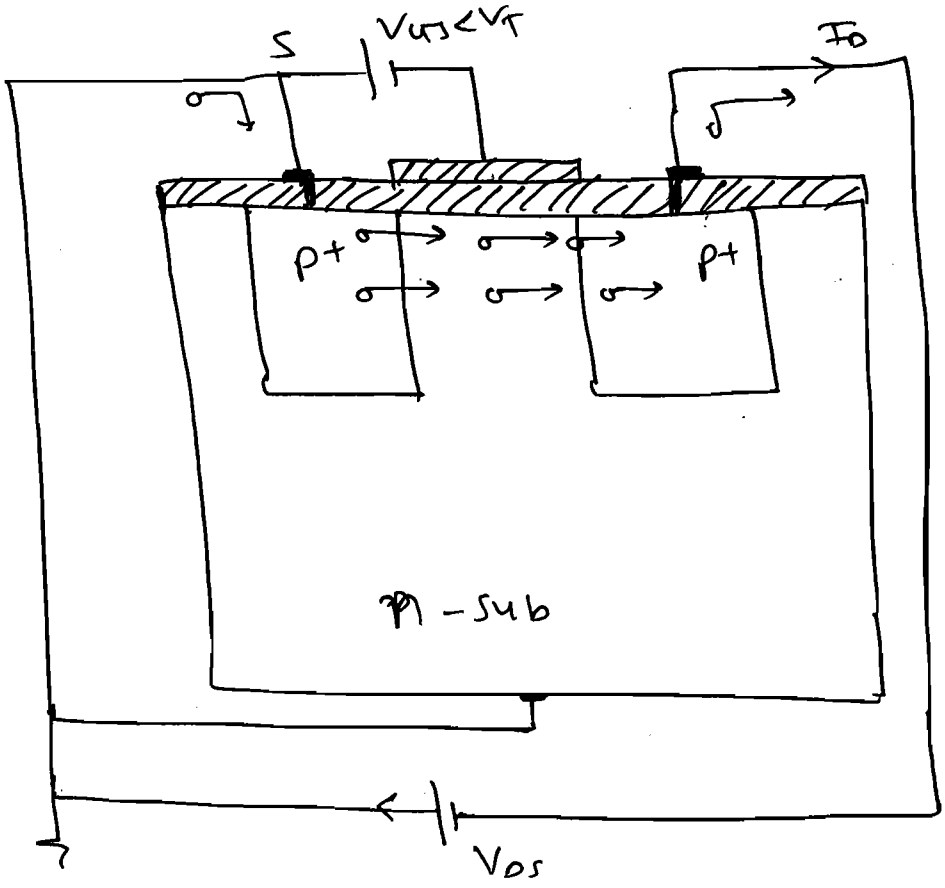


① $V_{GS} > V_T$: Cut-off:



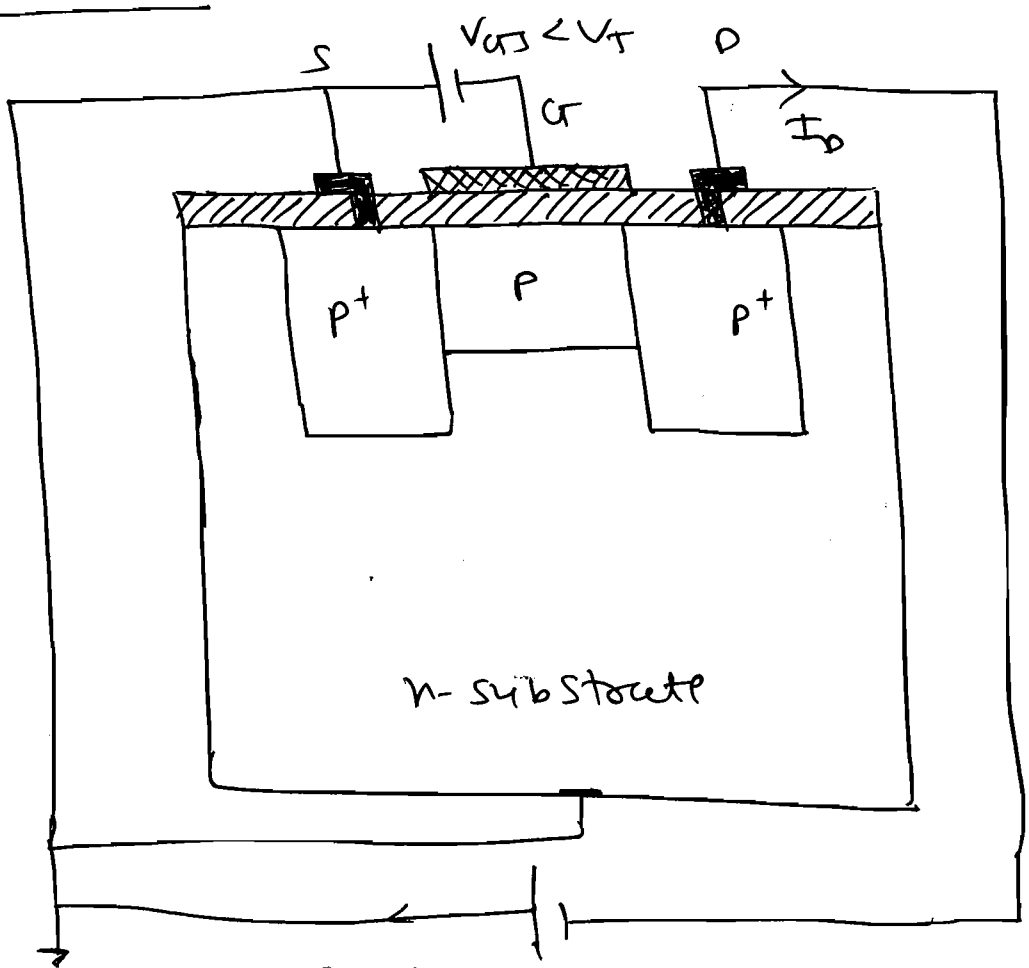
$|V_{GS}| < |V_T|$

(2) $V_{GS} < V_T$ & $V_{DS} > V_{GS} - V_T$: Linear.



$|V_{GS}| > |V_T|$ & $|V_{DS}| < |V_{GS} - V_T|$.

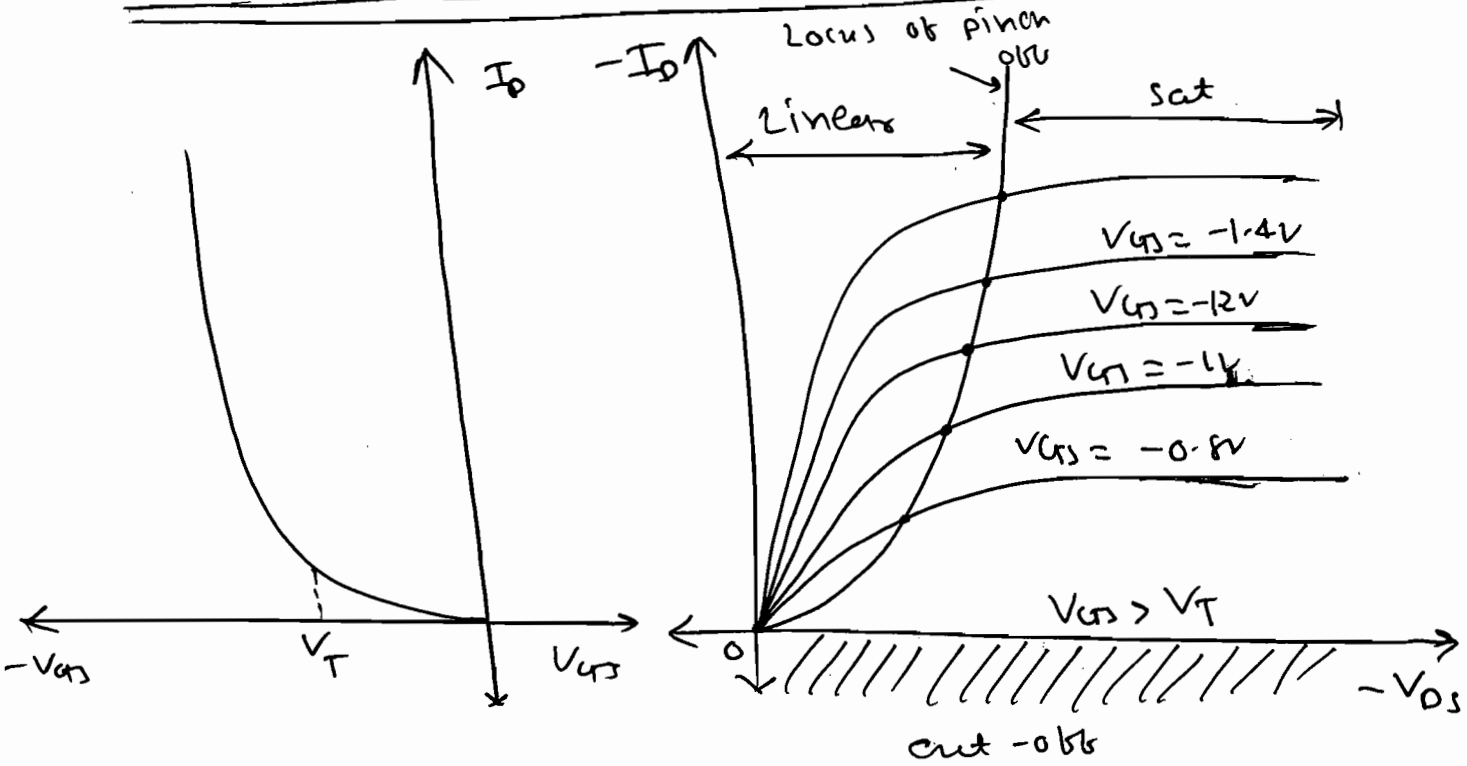
(3) $V_{GS} < V_T$ & $V_{DS} < V_{GS} - V_T$: Saturation.



$\Rightarrow |V_{GS}| < |V_T|$ & $|V_{DS}| > |V_{GS} - V_T|$.

$V_{DS} = -ve$, $V_{GS} = -ve$, $V_T = -ve$.

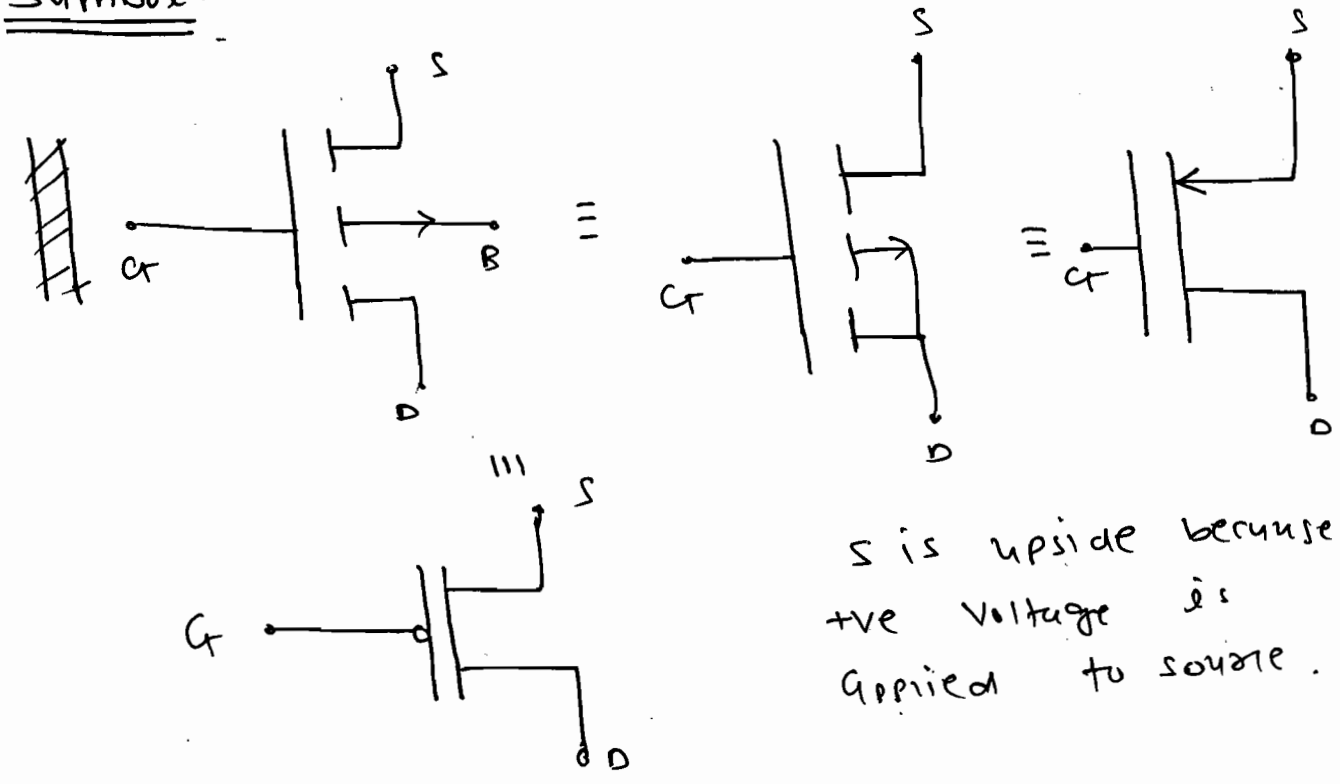
* Drain and Transfer Characteristics:



Transfer Characteristics

Drain Characteristics

* Symbol:



S is upside because +ve voltage is applied to source.

* Condition for pinch-off:

$\Rightarrow V_{DS} = V_{GS} - V_P$

V_{DS}: -ve, V_{GS}: -ve, V_P: -ve

$\Rightarrow V_{DS} > V_{GS} - V_P$: Linear

$V_{DS} < V_{GS} - V_P$: Sat.

*

	n-MOS	P-MOS
$V_{GS} = 0$	OFF	OFF
V_{GS} = +ve i.e. $(V_{GS} > V_T)$:	ON	OFF
V_{GS} = -ve i.e. $(V_{GS} < V_T)$:	OFF	ON.

*

n-MOS

① V_{DD}, G, $V_i = 0$, V_{GS} (+ −)

$V_{GS} = V_G - V_S = V_i - V_S = 0$

$\therefore$ (OFF)

② V_{DD}, G, $V_i = V_{DD}$, V_{GS} (+ −)

$V_{GS} = V_G - V_S = V_{DD}$

(ON)

P-MOS

① V_{DD}, V_{GS} − S, G, D, $V_i = 0$

$V_{GS} = V_G - V_S = 0 - V_{DD}$

$V_{GS} = -V_{DD} < V_T$

So, (ON)

② V_{DD}, V_{GS} − S, V_{GS}, D, $V_i = V_{DD}$

$V_{GS} = V_G - V_S$

$= V_{DD} - V_{DD} = 0$

So, (OFF)

* Imp Points to be remember:

⇒ P- Channel MOSFET operates with -ve gate voltages i.e. -Ve V_{GS} values.

⇒ Gate-to source voltage (i.e. V_{GS}) and Threshold voltage (V_T) are -ve for P-channel enhancement MOSFET.

⇒ P- Channel EMOSFET operates in enhancement mode for -ve V_{GS} values.

⇒ In descrete P- EMOSFET, substrate (or) Body (or) Bulk is connected to source terminal (or) V_{DD}. whereas in ICs it should be connected to most +ve values.

⇒ P- EMOSFET will be on for -ve V_{GS} values (i.e. $V_{GS} < V_T$) and it will be OFF for 0 or +V_{GS} values i.e. ($V_{GS} > V_T$)

⇒ Condition for pinch-off (or) saturation is $V_{DS} = V_{GS} - V_T$. and here, all are -ve.

⇒ For $V_{GS} > V_T$ (or) $|V_{GS}| < |V_T|$. P-MOSFET operates in cut-off region and its drain Current $I_D = 0$.

⇒ For $V_{GS} < V_T$ and $V_{DS} > V_{GS} - V_T$ (or)

$|V_{GS}| > |V_T|$ and $|V_{DS}| < |V_{GS} - V_T|$

it operates in linear region and its drain current

$$I_D = \mu_p \cdot C_{ox} \cdot \frac{W}{L} \left[(V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

(V_{GS}: -ve, V_T: -ve)

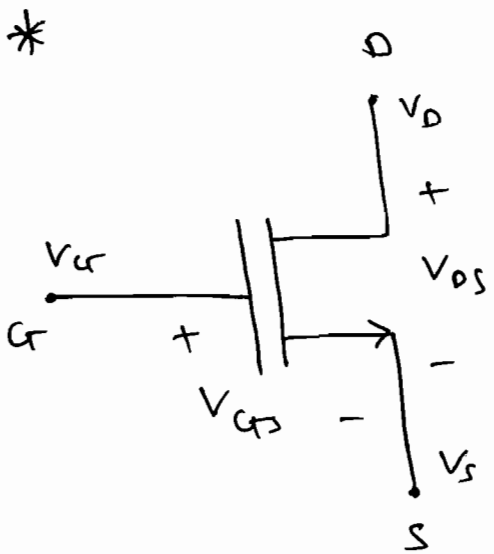
μ_p: mobility of holes.

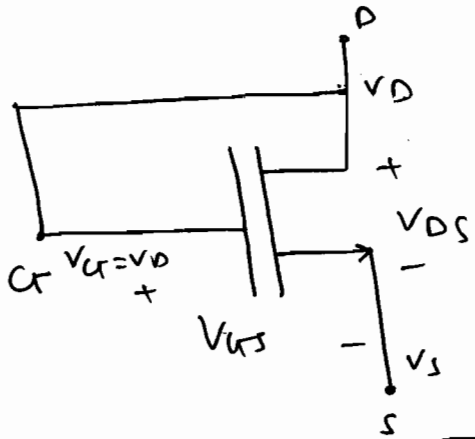
$\Rightarrow$ For $V_{GS} < V_T$ & $V_{DS} \leq V_{GS} - V_T$ (or) $|V_{GS}| > |V_T|$ & $|V_{DS}| \geq |V_{GS} - V_T|$. it operates in saturation region and its drain current,

$$I_D = \frac{1}{2} \mu_p \cdot C_{ox} \cdot \frac{W}{L} [V_{GS} - V_T]^2$$

(V_{GS}: -ve, V_T: -ve)

*



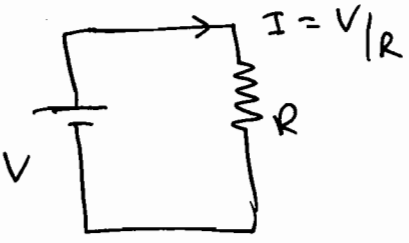


→ if $V_G = V_D \Rightarrow V_{GS} = V_{DS}$

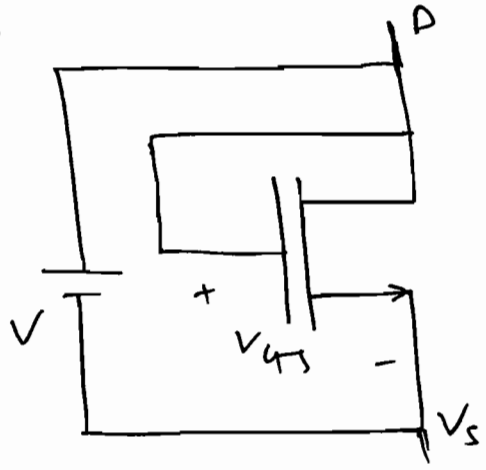
→ if $V_{GS} = V_{DS}$ & $V_{GS} > V_T \Rightarrow$ Sat

$V_{GS} = V_G - V_S$

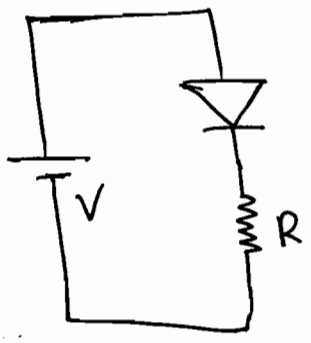
$V_{DS} = V_D - V_S$



$\Rightarrow$



$\equiv$

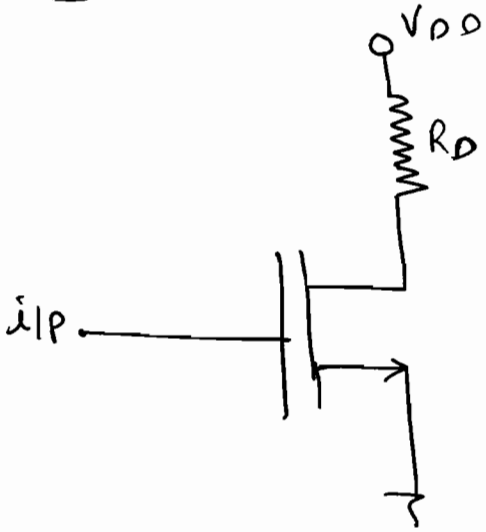


$V_{GS} = V > V_T$

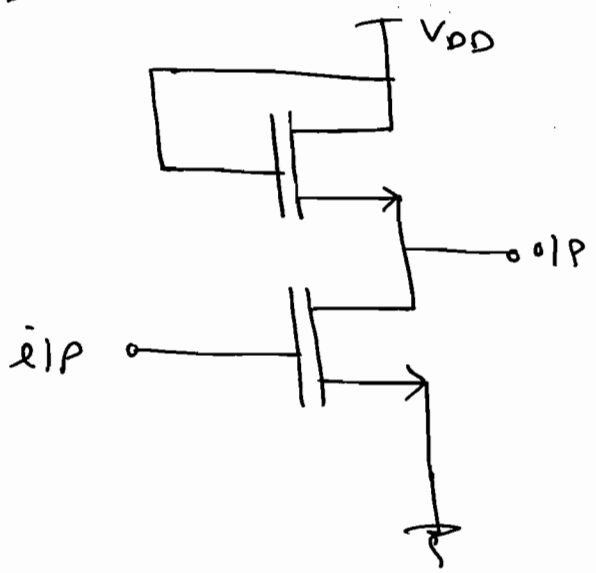
then I will flow.

☆ Types of Load:

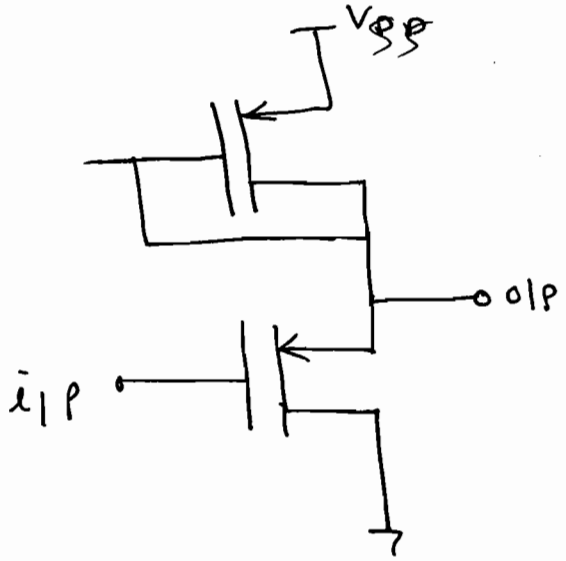
① Resistive Load:



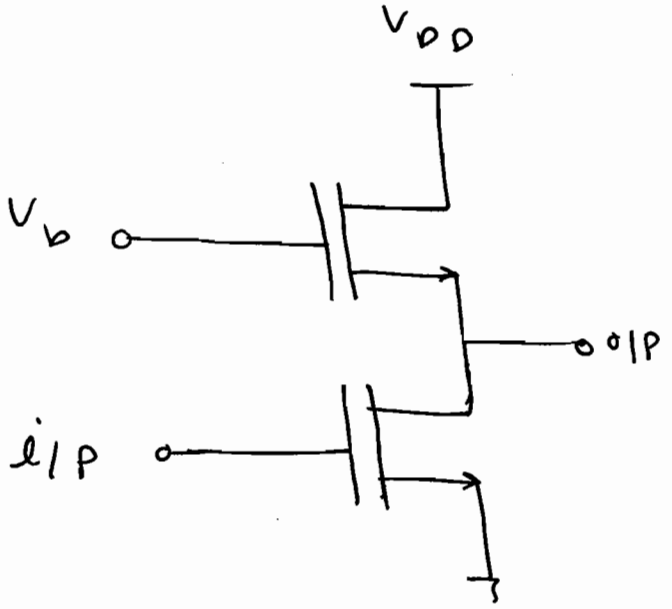
(ii) Diode connected Load:



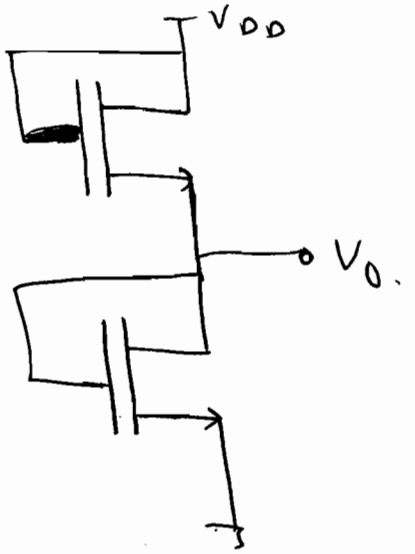
&



③ Current-Source Load:



Q Find V_o in the given figure.



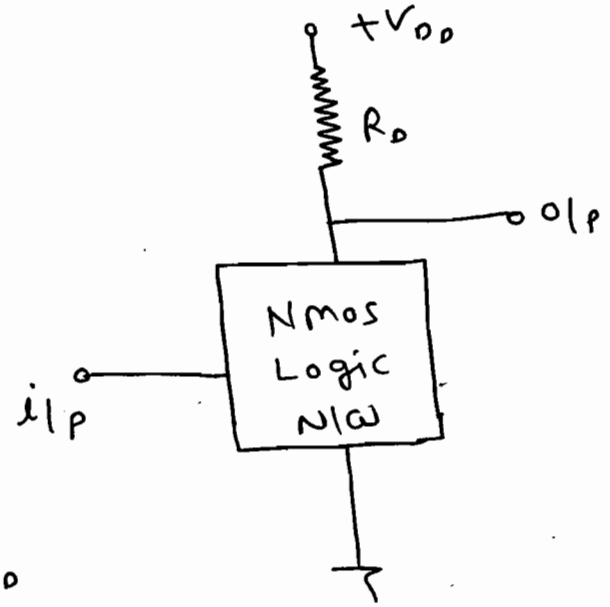
Soln: Both are n-channel and same parameters. So, Both are act as a same Resistor. Hence $V_o = \frac{V_{DD}}{2}$.

✡ CMOS (complementry MOS):

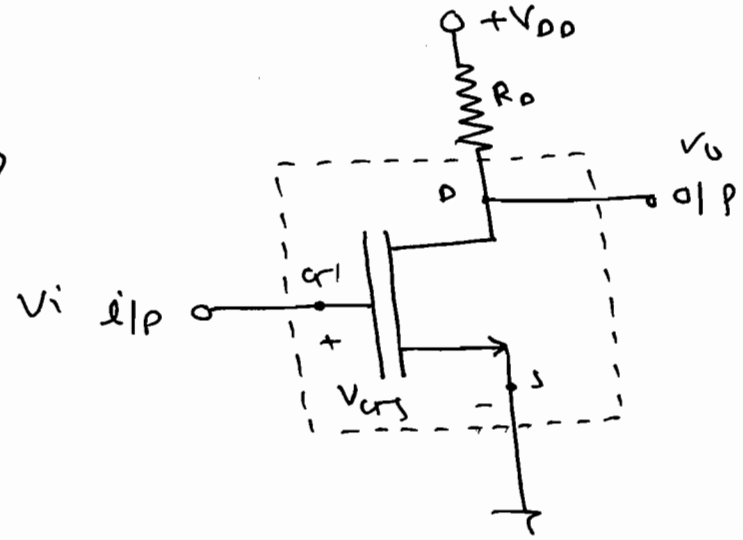
* n-MOS:

⇒ Inverter:

A	Y = $\bar{A}$
0	1
1	0



⇒

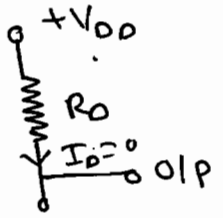


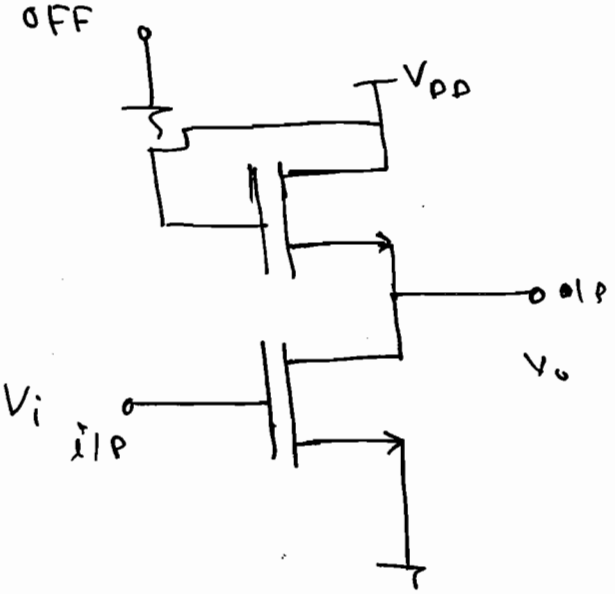
(i) $\boxed{V_i = 0}$

$V_{GS} = V_G - V_S = V_i - 0$

$V_{GS} = 0$

⇒ $\boxed{OFF}$



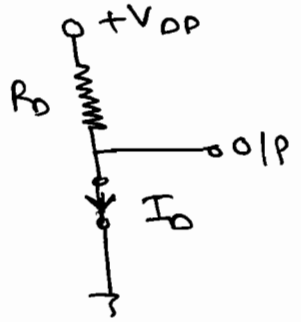


⇒

(ii) $\boxed{V_i = +V_{DD}}$

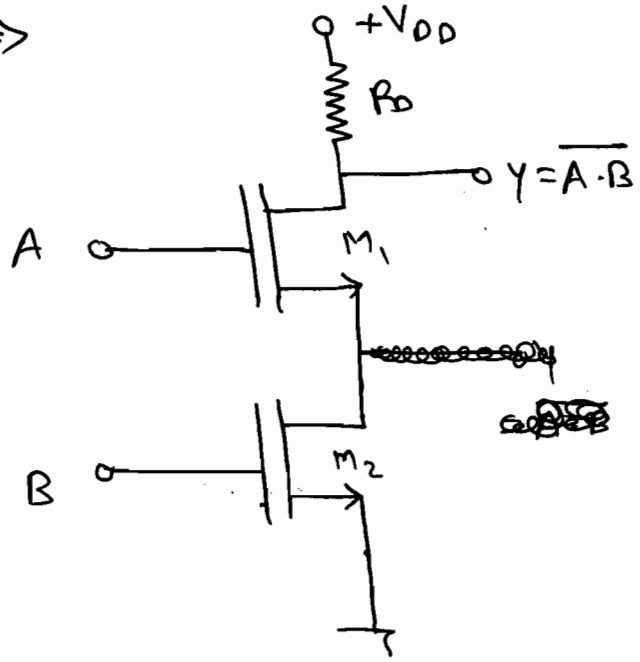
$V_{GS} = V_G - V_S = V_i - 0$

$V_{GS} = V_{DD}$ ⇒ $\boxed{ON}$



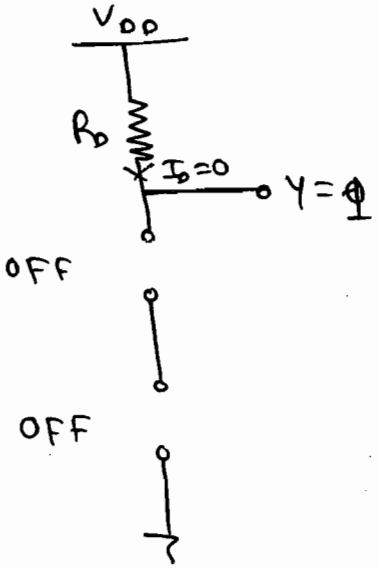
* 2- Input NAND Gate:-

⇒

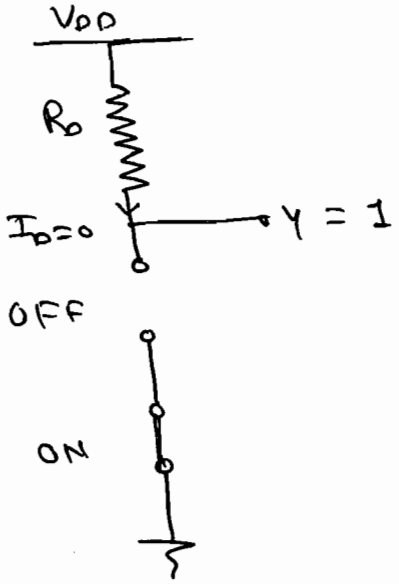


A	B	F = $\overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

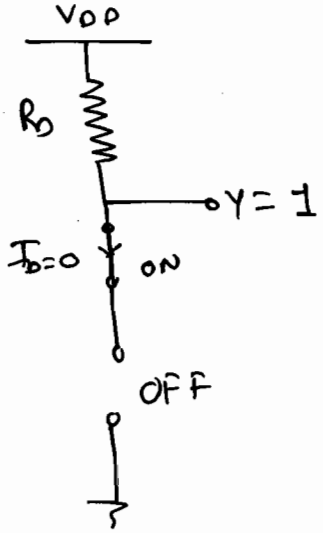
⇒ (i) V_i, A = 0, B = 0.



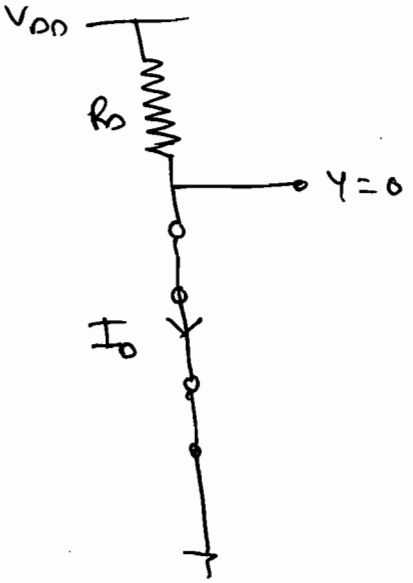
(ii) A = 0, B = 1.



(iii) A = 1, B = 0

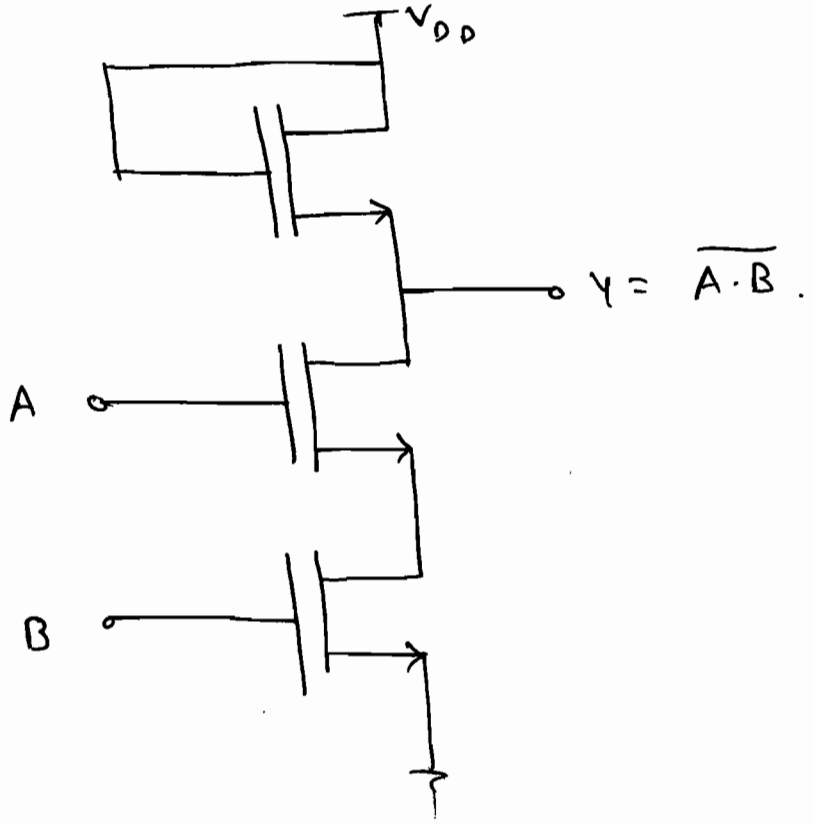


(iv) A = 0, B = 1



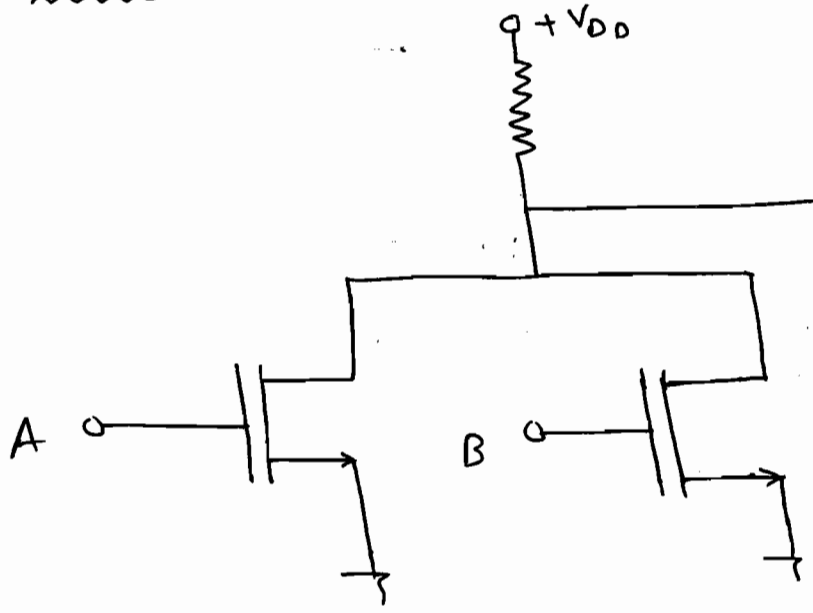
⇒ Replace R_D by one more nmos.

⇒



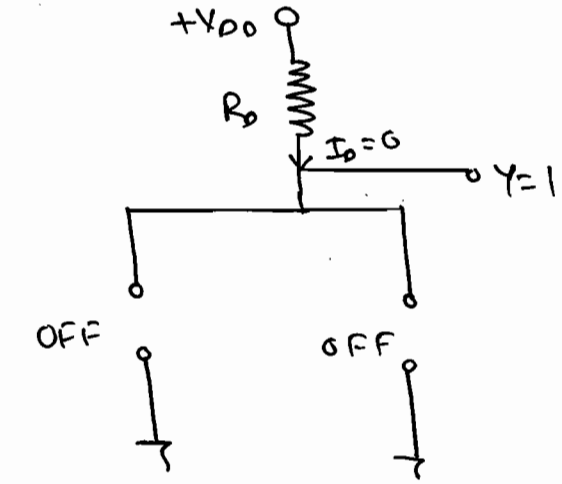
* 2-input NOR Gate:

⇒

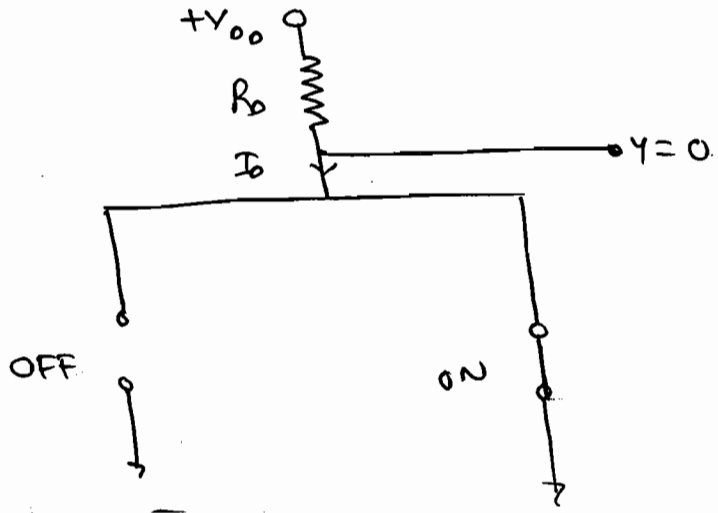


A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

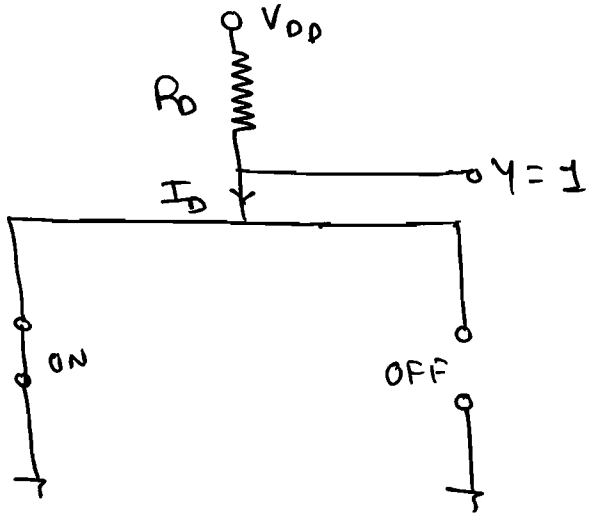
(i) A = 0, B = 0.



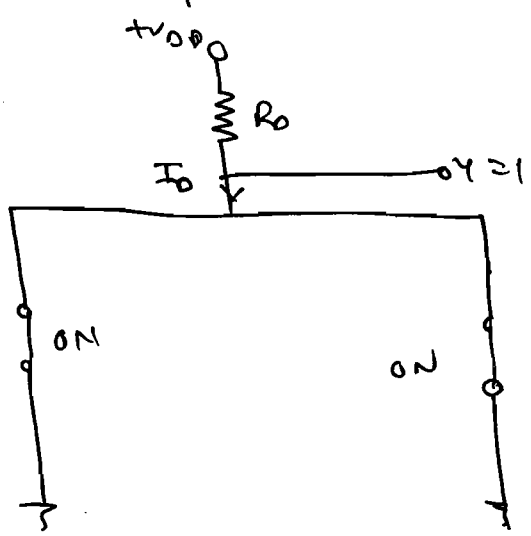
(ii) A = 0, B = 1.



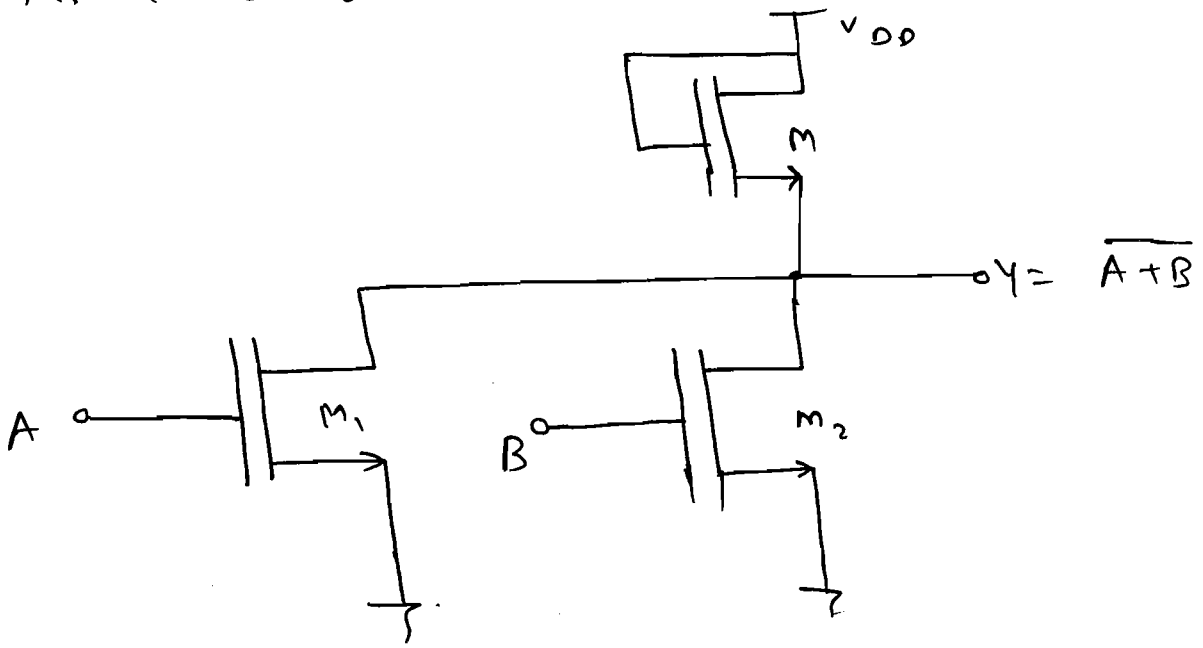
(iii) $A=1, \quad B=0$



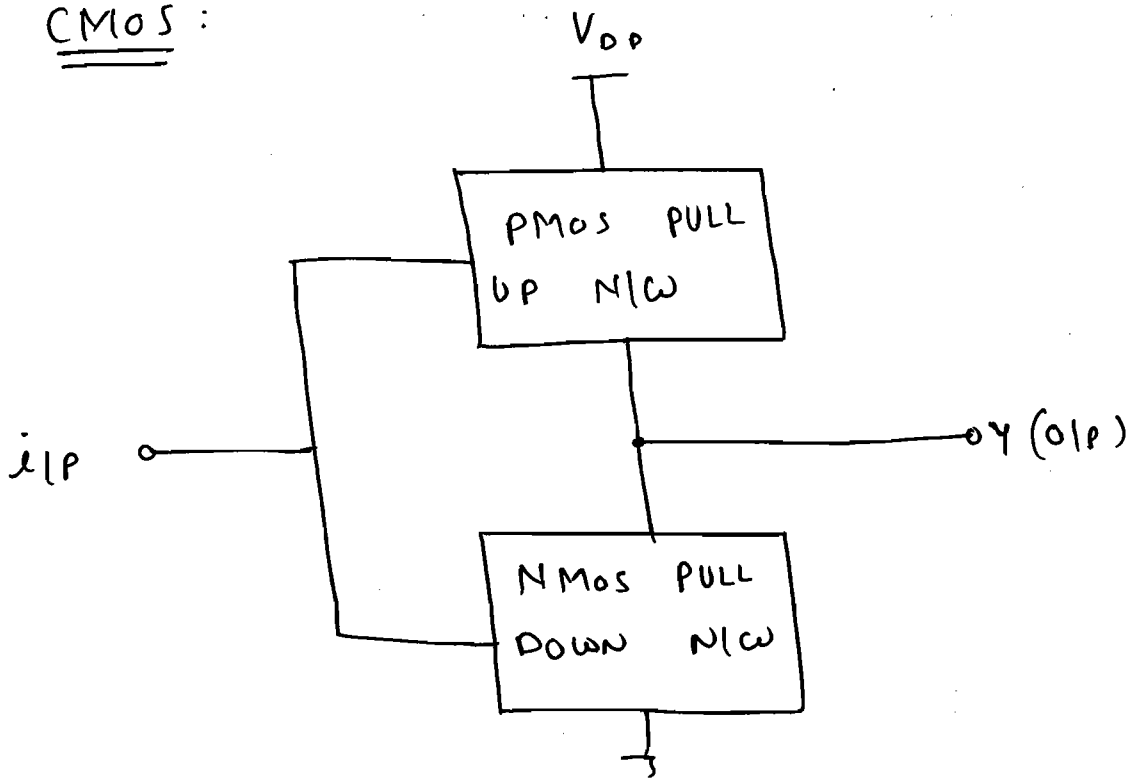
(iv) $A=1, \quad B=1$



$\Rightarrow$ Replace R_D by one more NMOS.

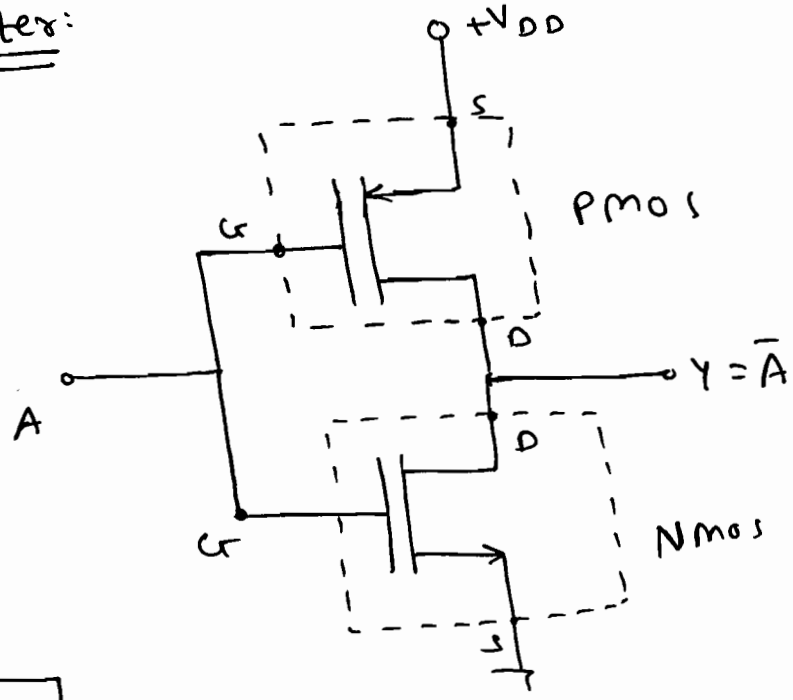


* CMOS:

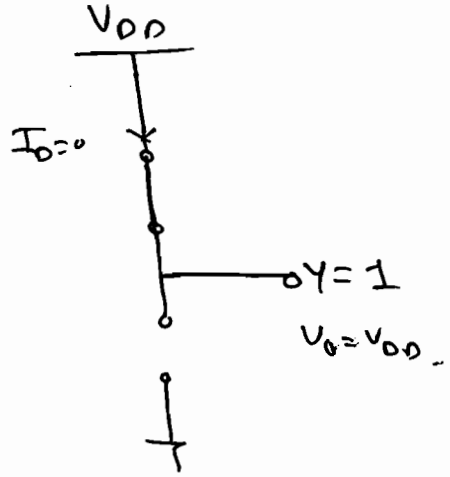


* Inverter:

$\Rightarrow$



(i) $V_i = 0$



NMOS

$V_{GS} = V_G - V_S$

$= V_i - 0$

$V_{GS} = V_i = 0$

OFF

PMOS

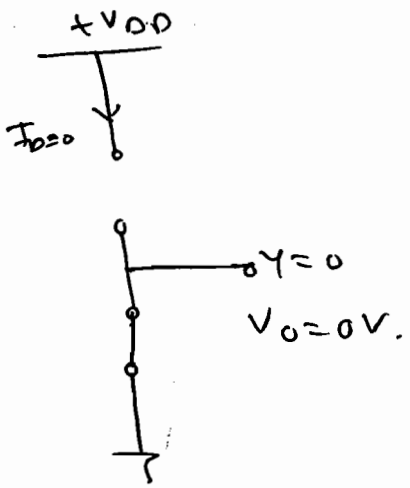
$V_{GS} = V_G - V_S$

$= V_i - V_{DD}$

$V_{GS} = -V_{DD}$

ON

(ii) $V_i = +V_{DD}$



NMOS

$V_{GS} = V_G - V_S$

$= V_{DD} - 0$

$V_{GS} = V_{DD}.$

$\Rightarrow$ ON

PMOS

$V_{GS} = V_G - V_S$

$= V_{DD} - V_{DD}$

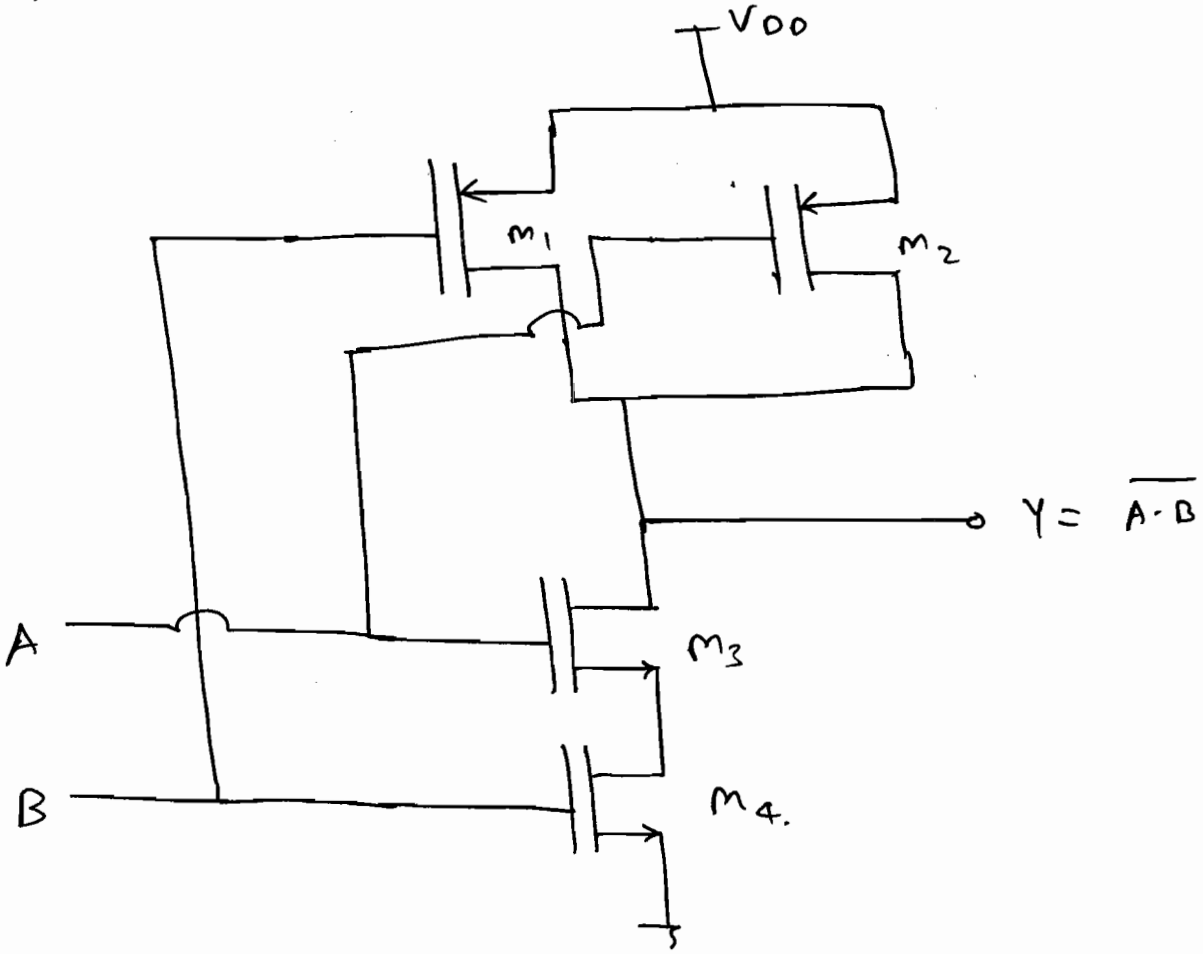
$V_{GS} = 0$

$\Rightarrow$ OFF

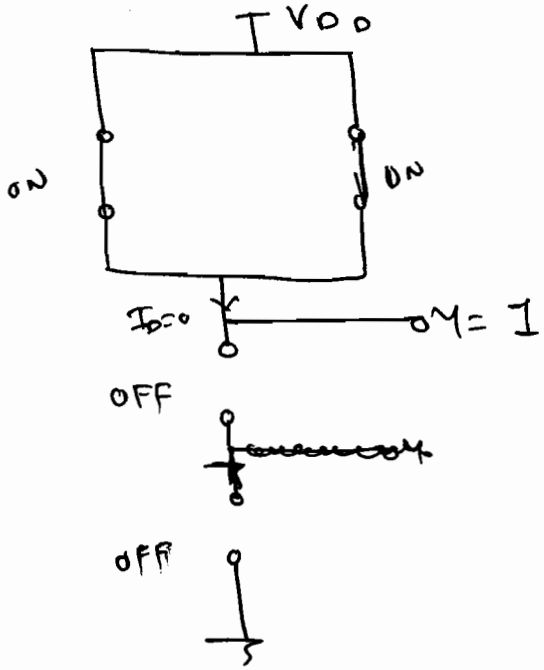
$\Rightarrow$ Here in both the case Ideally I_D Current is zero and ideally power dissipated is zero. But practically some small o/p Resistance So, some small power dissipated in T_x. But is very small Compare to other technology.

* 2 ip NAND gate:

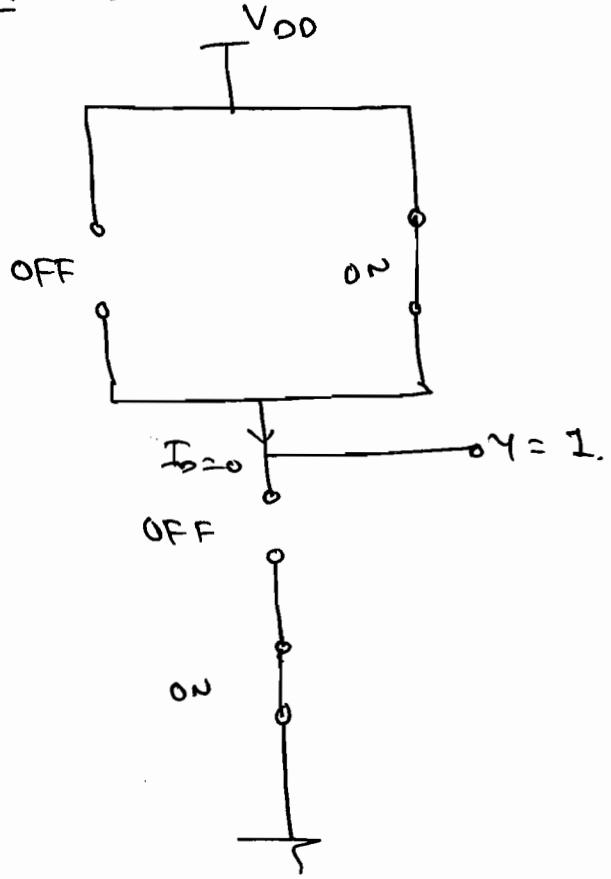
⇒



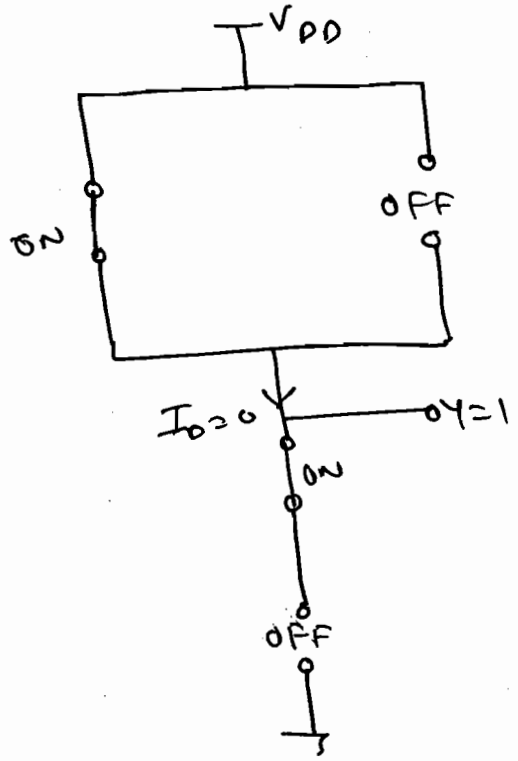
Case -(i) A = 0, B = 0.



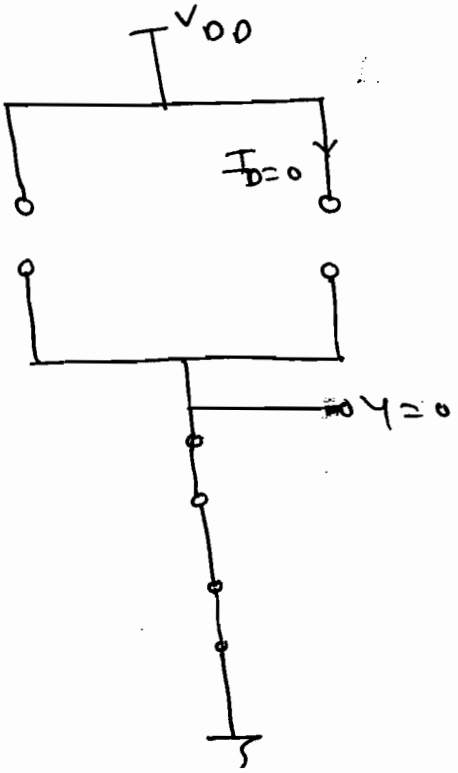
Case -(ii) A = 0, B = 1



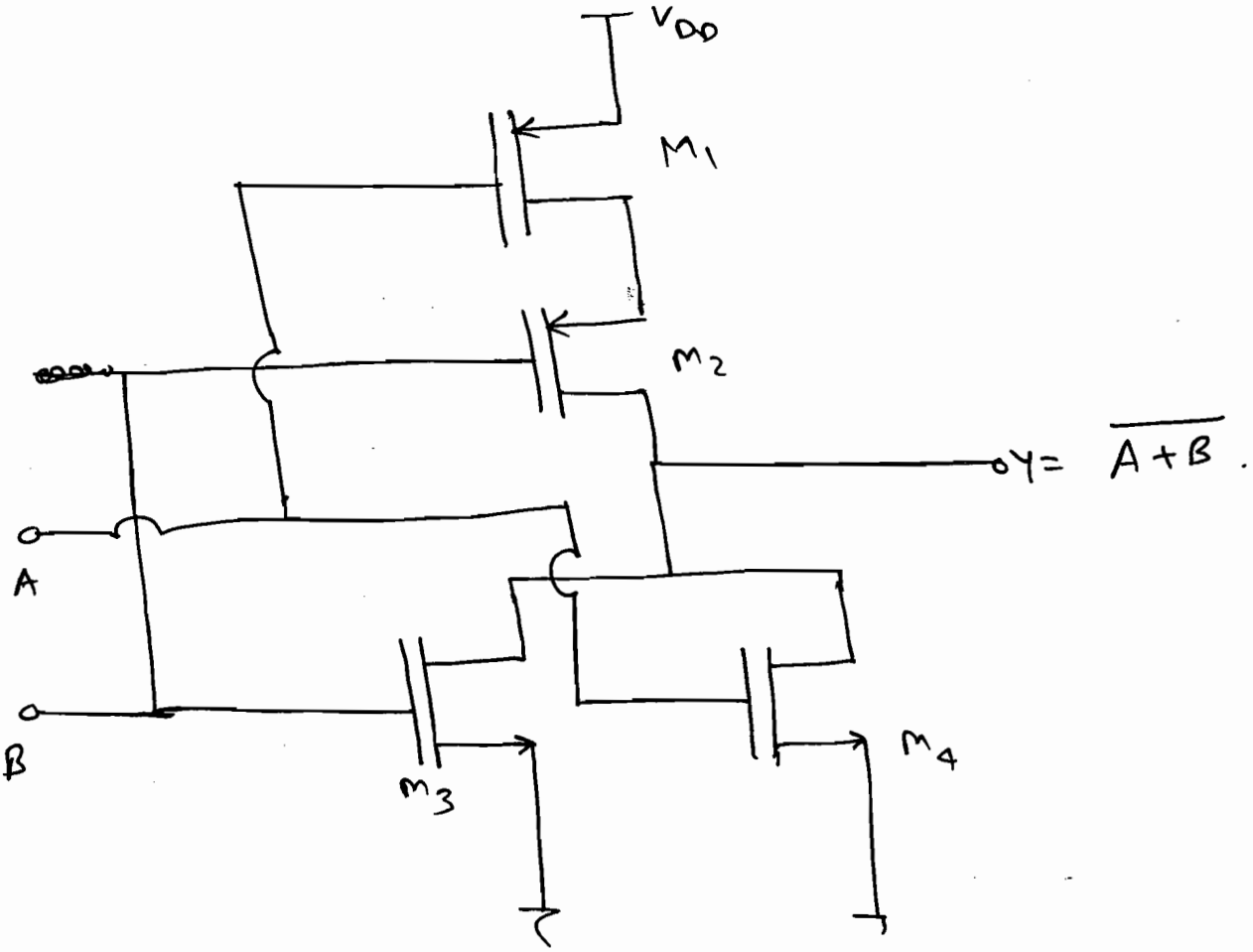
(iii) $A=1,\ B=0$



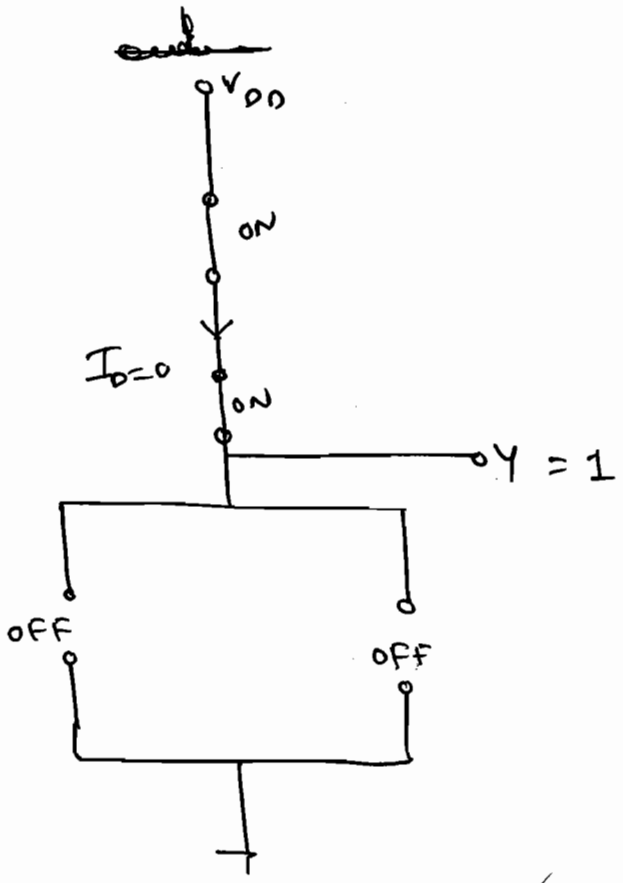
(iv) $A=1,\ B=1$



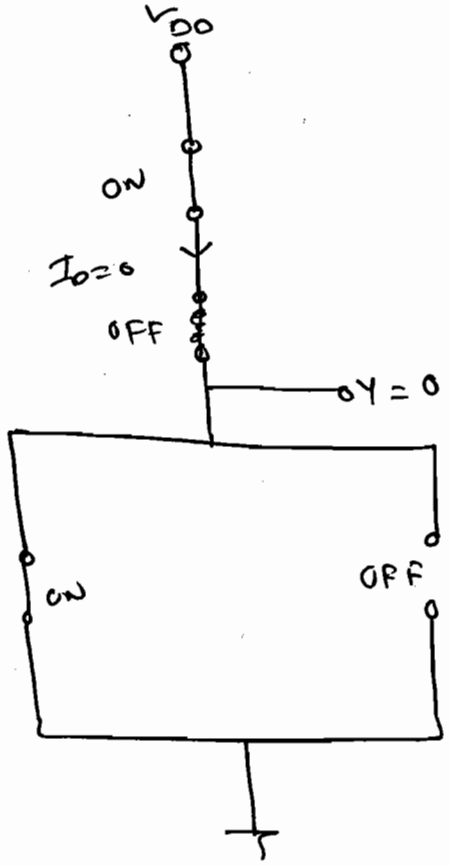
* 2- input NOR Gate:



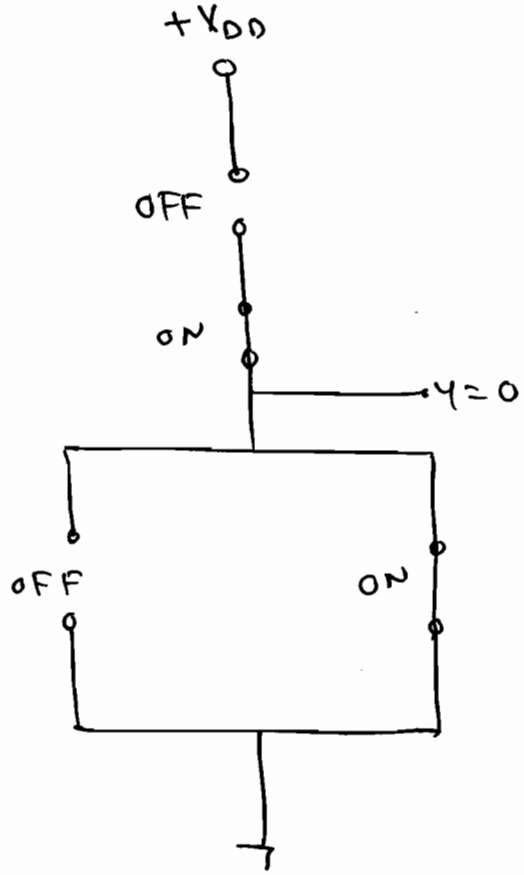
Case - (i): A=0, B=0



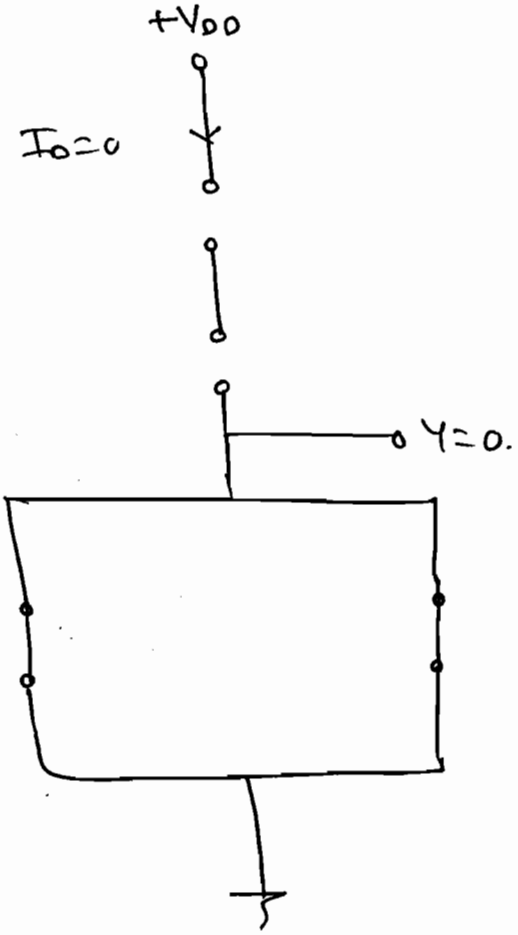
case - ii : A=0, B=1.



Case - (iii) A=1, B=0



case (iv) A=1, B=1



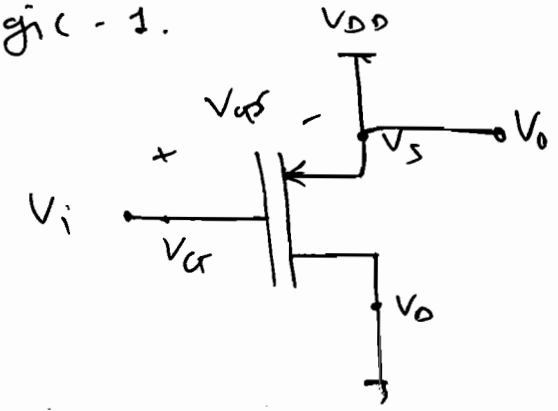
IMP Concept:

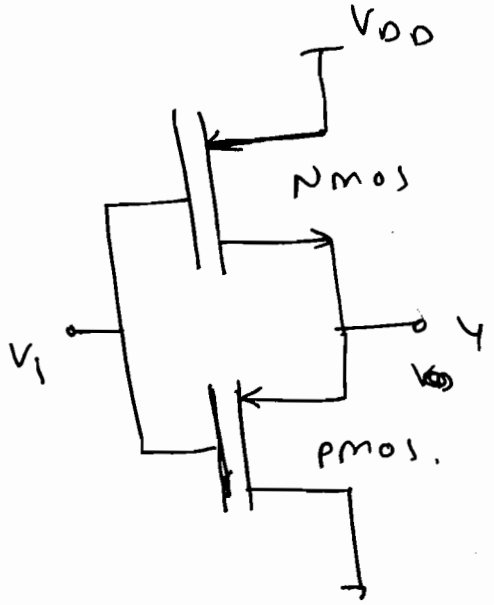
=> Why pmos is connected to upside & Nmos is Connected to Down in CMOS?

Ans:

=> Pmos Transistor passes Logic -1 without Distortion. But it passes Logic - 0 with distortion. Therefor pmos transistors always connected to V_{DD} (or) pulled up to pass Logic - 1.

=>





=> if $V_i = 0$. => V_o should be zero (or).

i.e. pmos is in ON state.

$\therefore$ for that $V_{GS} < V_T$.

let, $V_T = -0.7\,V$.

$\therefore V_G - V_S < V_T$.

$\therefore 0 - V_o < V_T$.

$\therefore V_o > V_T$.

$\therefore |V_o| > |V_T|$.

i.e. $V_o > 0.7\,V$.

So, instead of getting '0'. we get 0.7.

So, distortion will occurs.

Now, Let, $V_i = +V_{DD}$. $\Rightarrow$ Pmos is OFF and V_o should be $+V_{DD}$.

$\therefore V_{GS} = V_G - V_S$

$\therefore V_{GS} = V_{DD} - V_{DD} = 0$

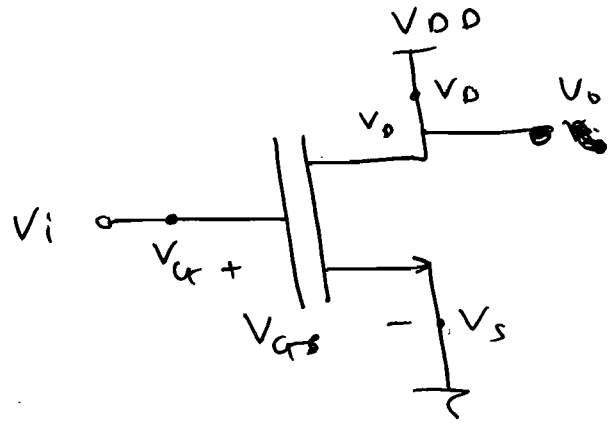
$V_{GS} = 0 \Rightarrow$ ~~$V_S = V_{DD}$~~. Pmos is OFF and

$V_S = V_o = +V_{DD}$ perfect.

So, Pmos passes Logic '1' without distortion and passes Logic '0' with distortion.

$\Rightarrow$ Nmos:

$\rightarrow$ Nmos Transistor passes Logic-0 without distortion and passes Logic-1 with distortion. Therefore Nmos Transistor always Connected to ground (or) pulled down to pass Logic-'0'.



$\Rightarrow$ Inorder to get $V_o = +V_{DD}$, $V_i = 0$. $\Rightarrow$ in Cut-off

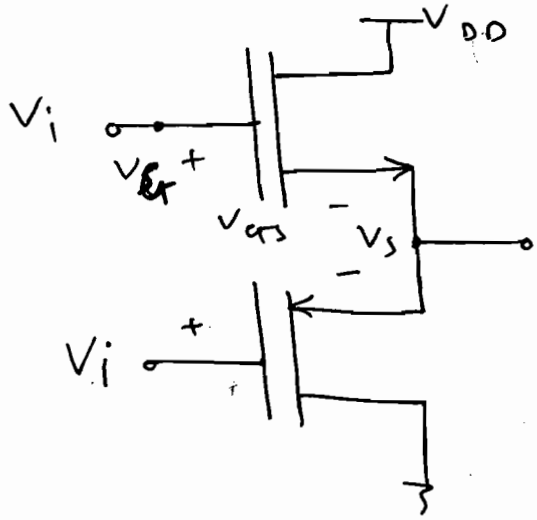
But for Cut-off $V_{GS} < V_T$. let $V_T = 0.7V$

$\therefore V_G - V_S < 0.7$

$\therefore V_G < 0.7$

So, V_i should be > 0.7.

=> Now, if Nmos is Connected to up-side then,



=> Now, if $V_i = 0$ then $V_S = V_o = +V_{DD} = +5V$ for inverter.

in order to get $V_S = V_o = +V_{DD} = +5V$ Nmos should be in ~~cut off~~ Sat.

$\therefore$ $V_{GS} \geq V_T$, Let $V_T = 0.7V$.

$\therefore$ $V_G - V_S \geq 0.7$.

$\therefore$ $0 - V_S \geq 0.7$.

$\therefore$ $-5 > 0.7$ → not possible

~~So, we get $V_o = 4.3$ instead of V_{DD}.~~

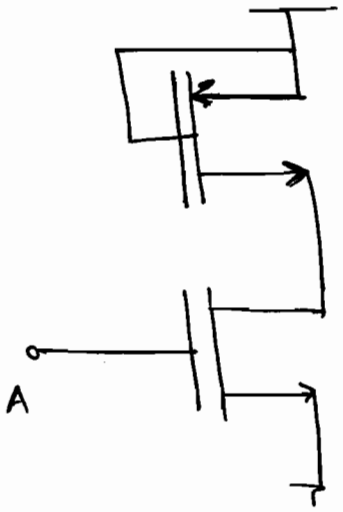
~~So get get distortion.~~ n-mos is OFF.

=> So, Nmos Transistor passes Logic-0 without distortion. But it passes Logic-1 with distortion. Therefore Nmos Transistor always Connected to ground (or) pulled down to pass Logic-0.

☆ Inverter:

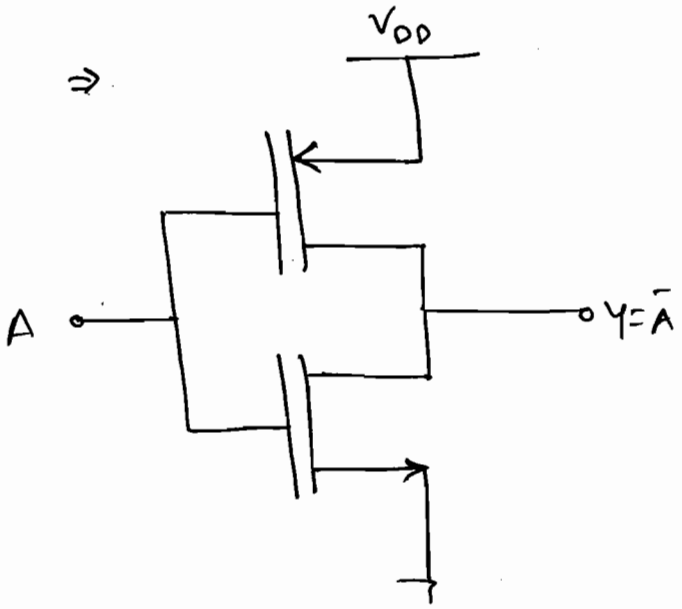
n-MOS

⇒



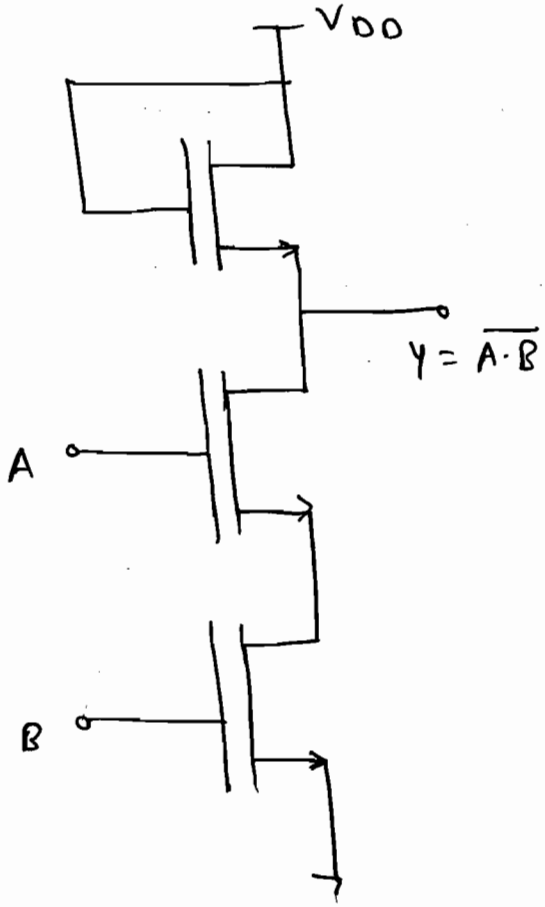
Cmos:

⇒

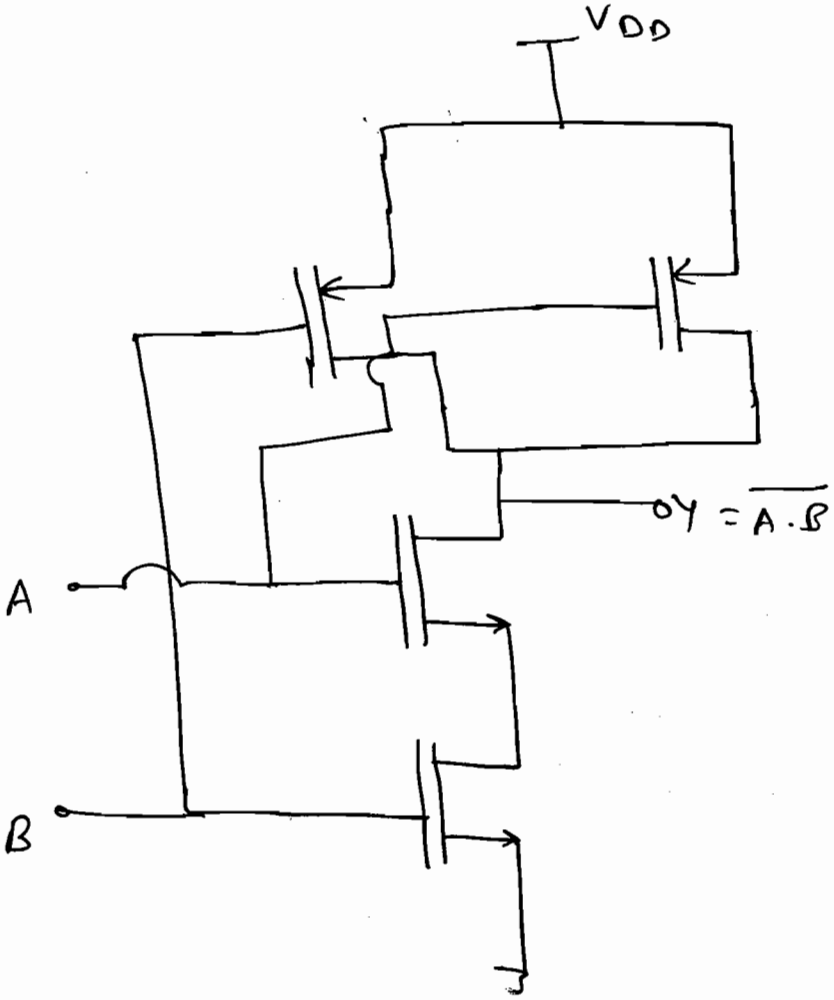


☆ 2 i/p NAND gate:

n-MOS

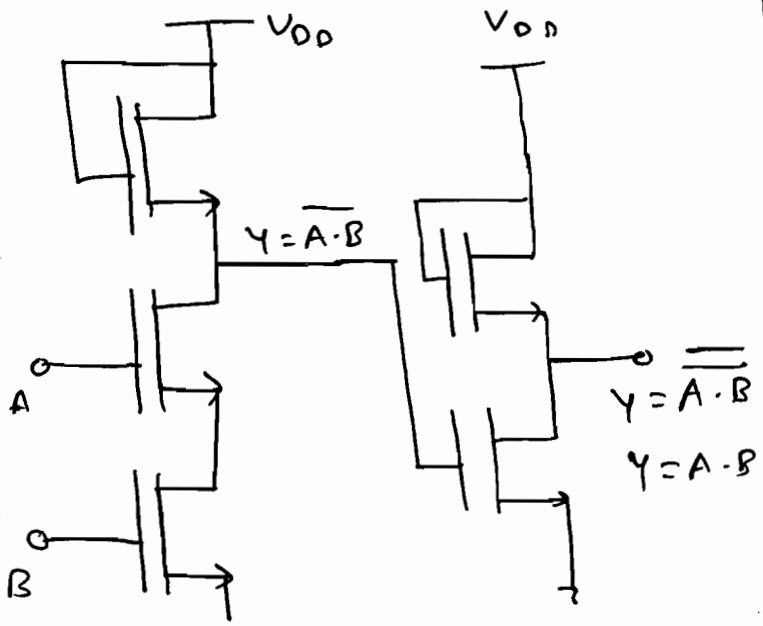


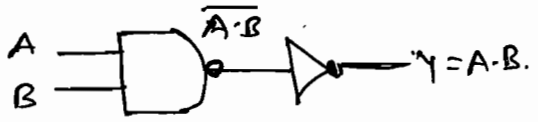
Cmos:



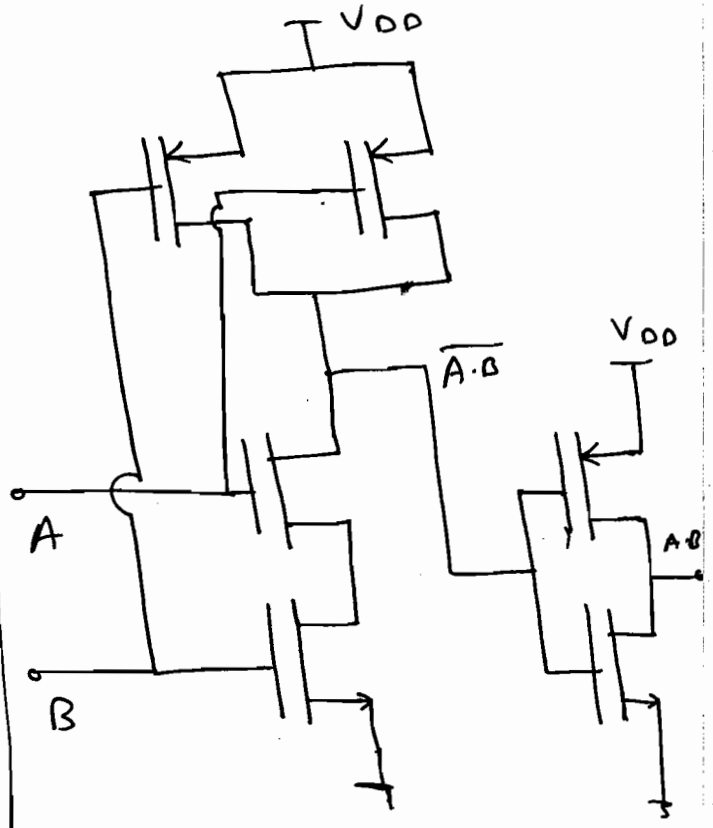
* 2- i/p AND Gate:

Nmos



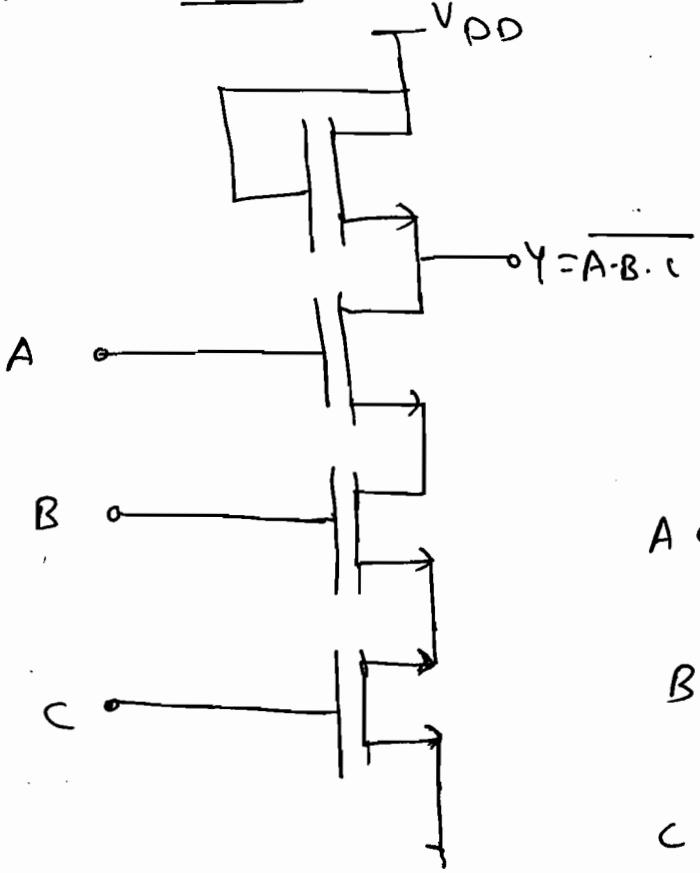


Cmos:

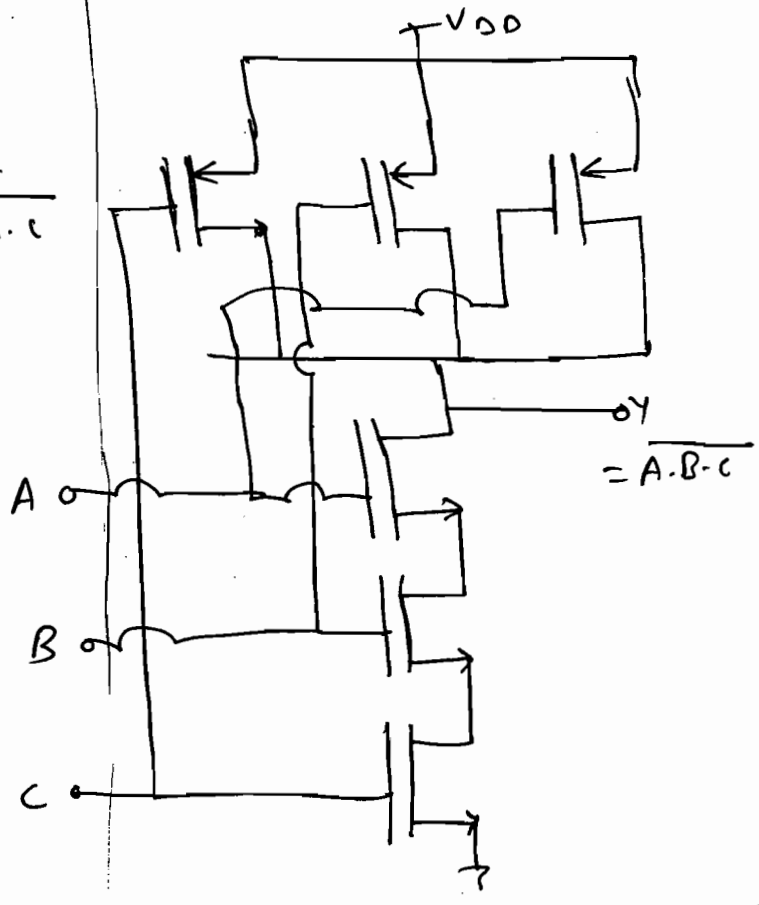


* 3- i/p NAND Gate:

⇒ Nmos:

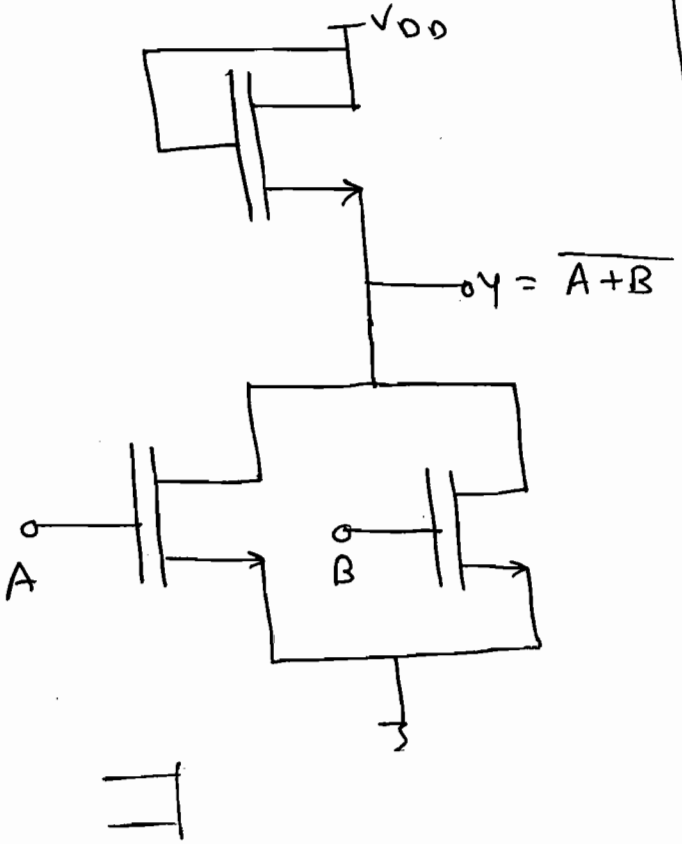


CMOS

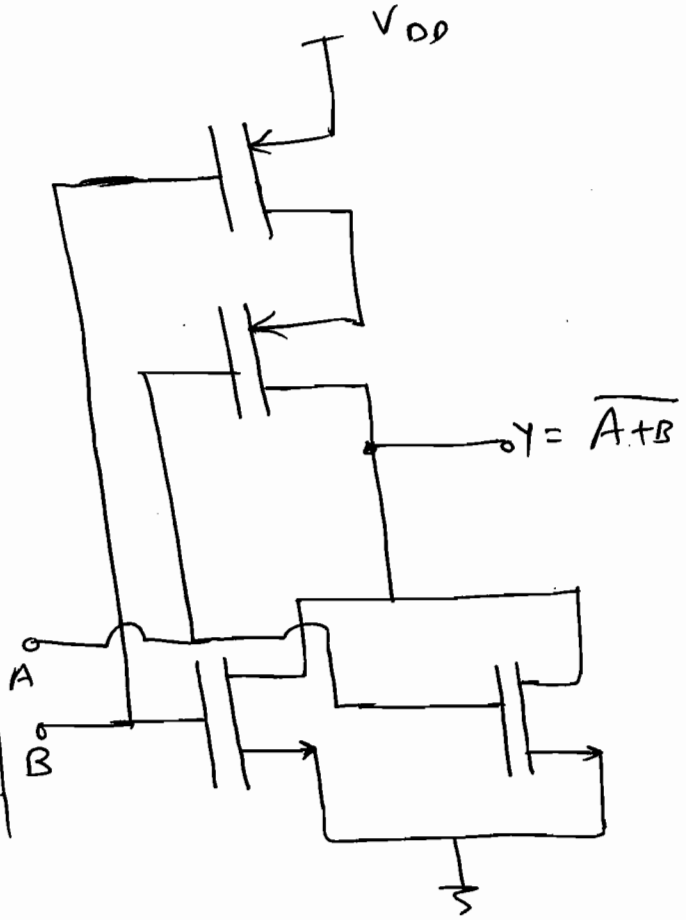


* 2 i/p NOR gate:

NMOS

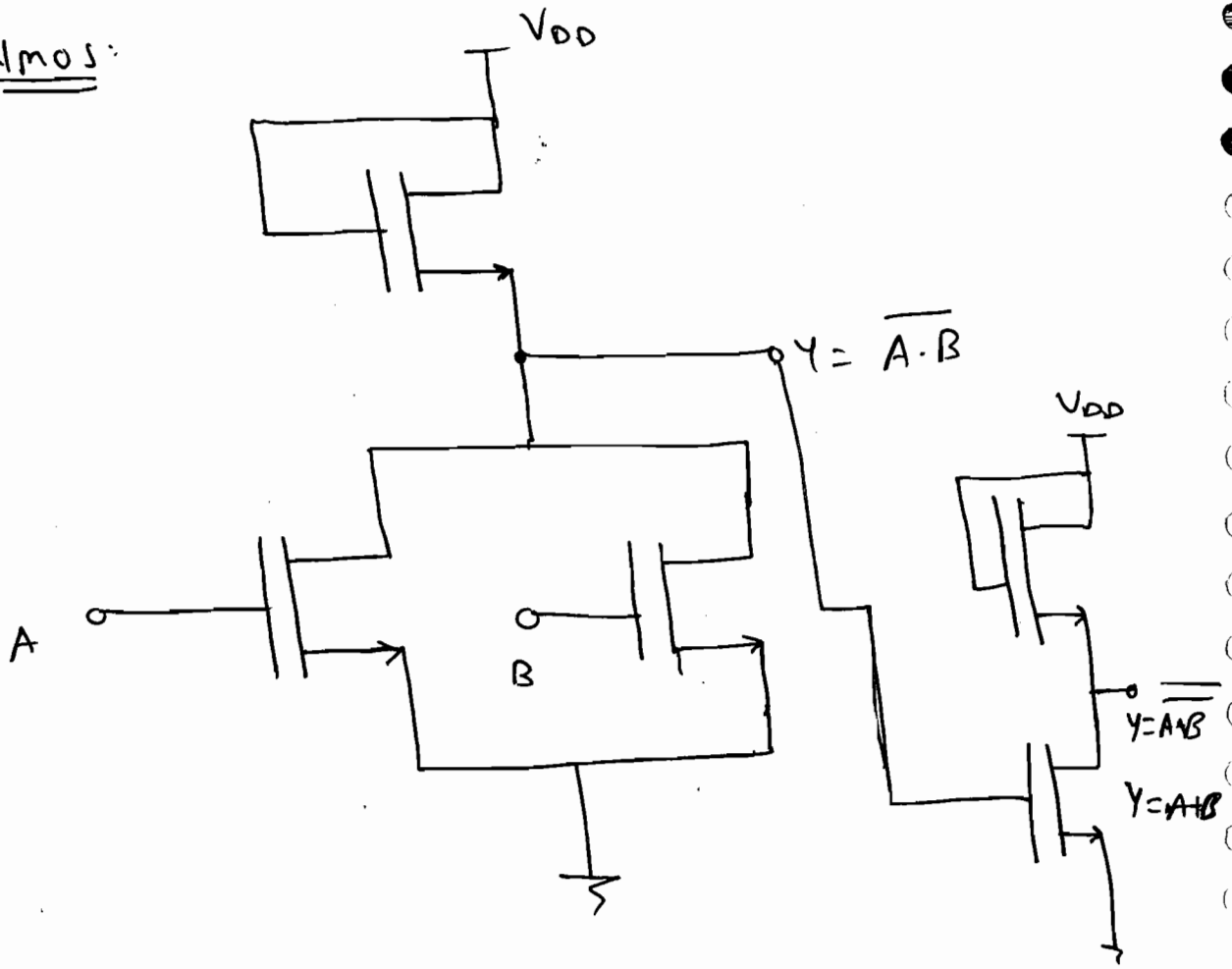


CMOS

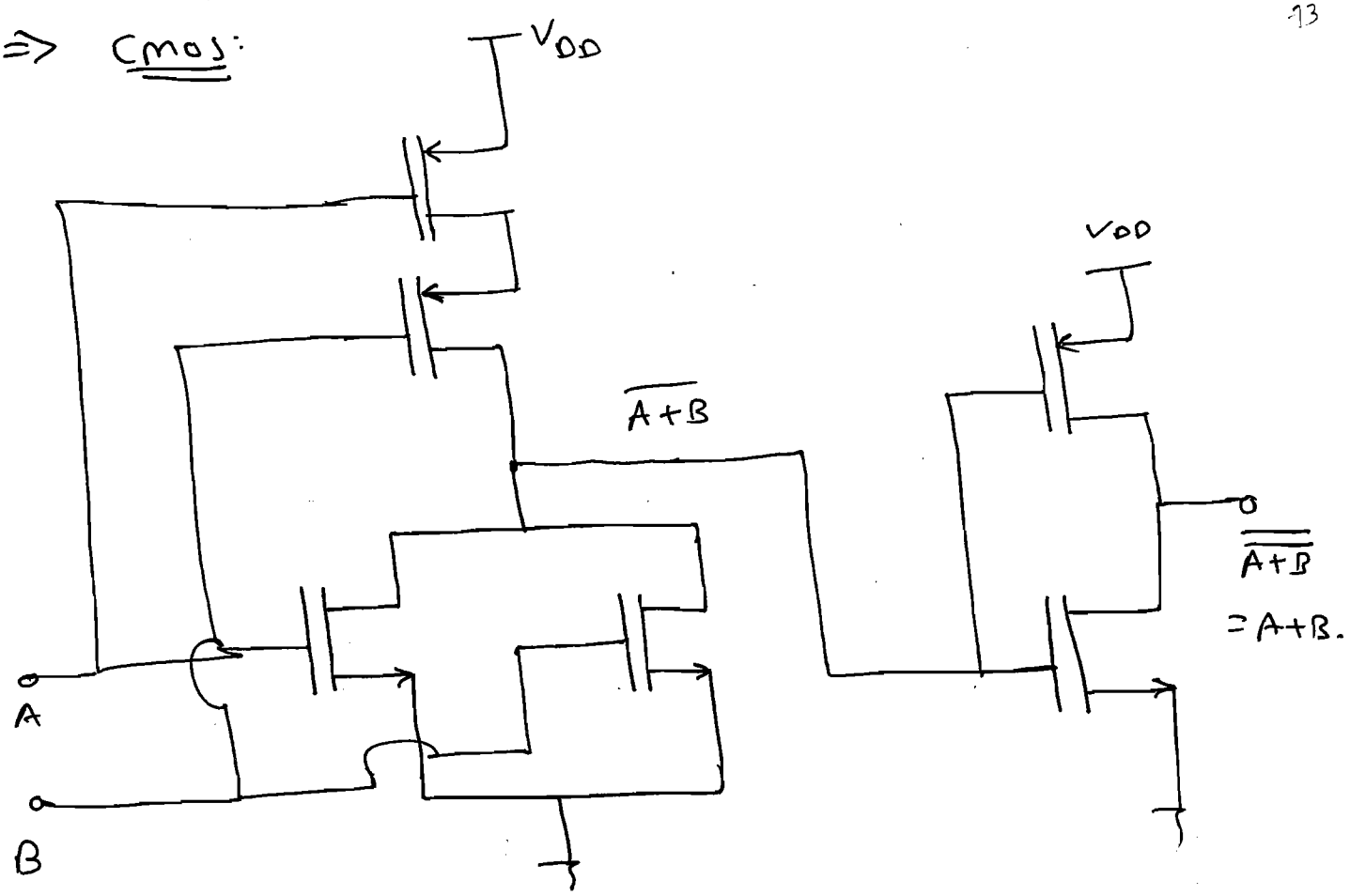


* 2 i/p OR gate:

NMOS:

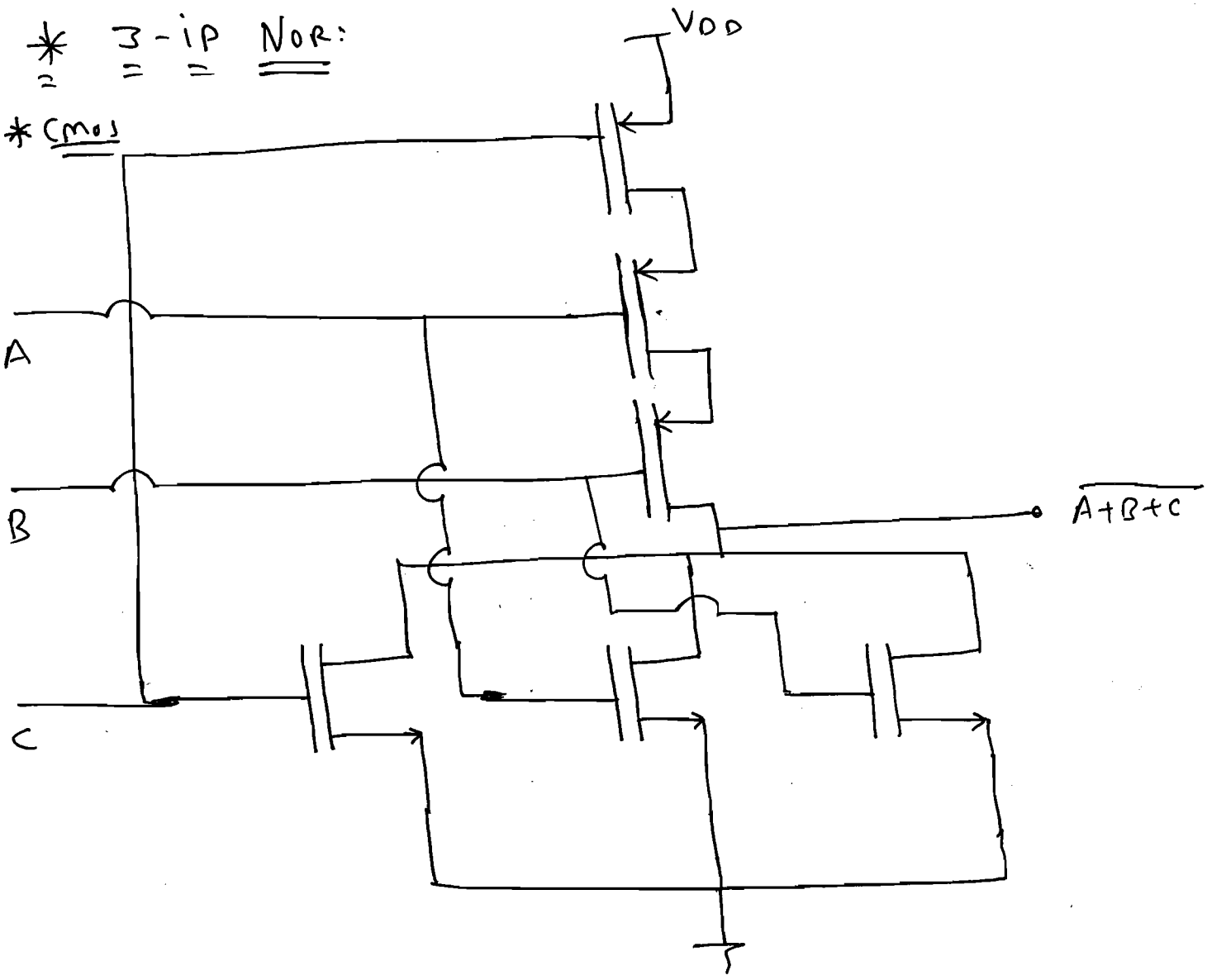


⇒ CMOS:

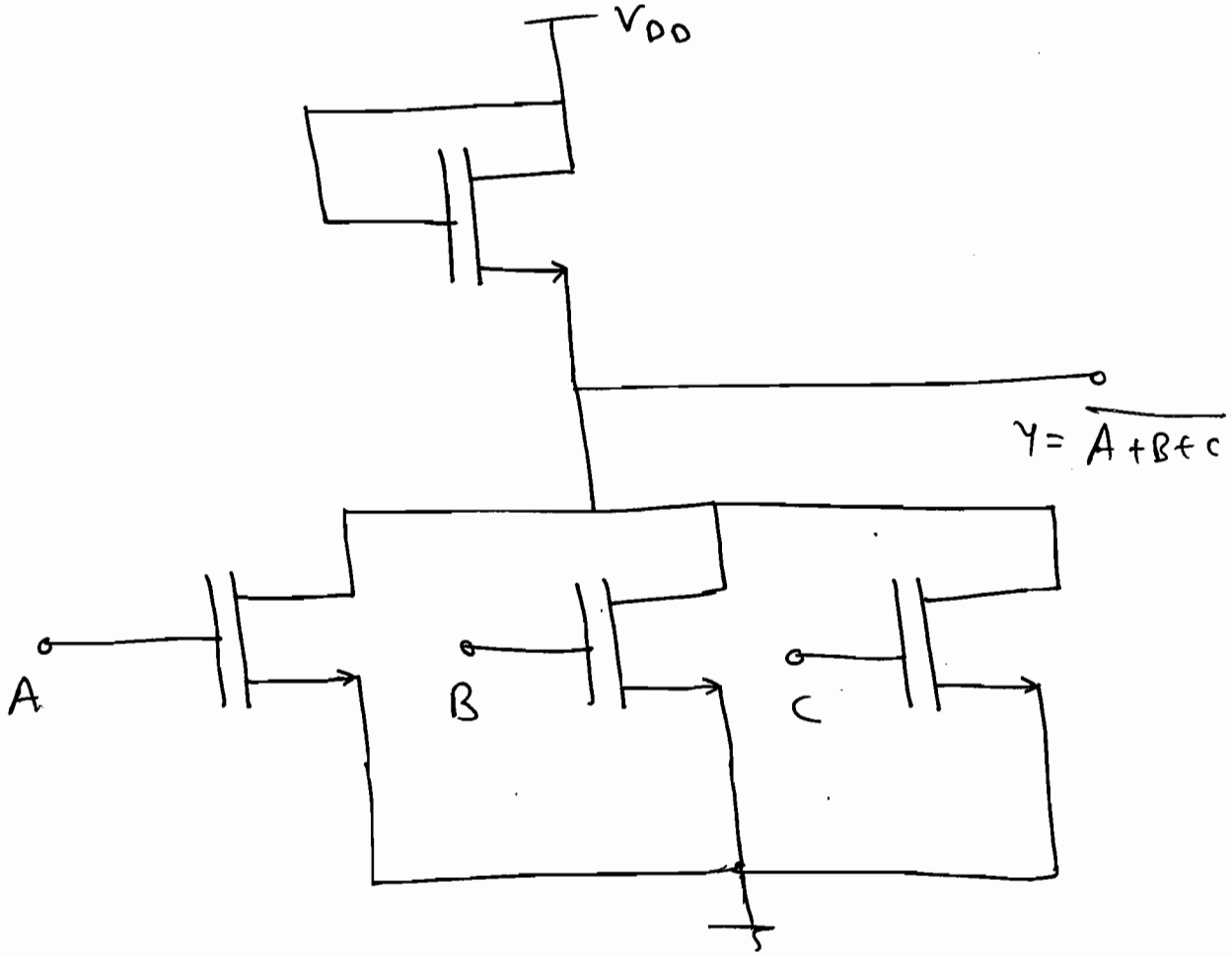


* 3-ip NOR:

* CMOS



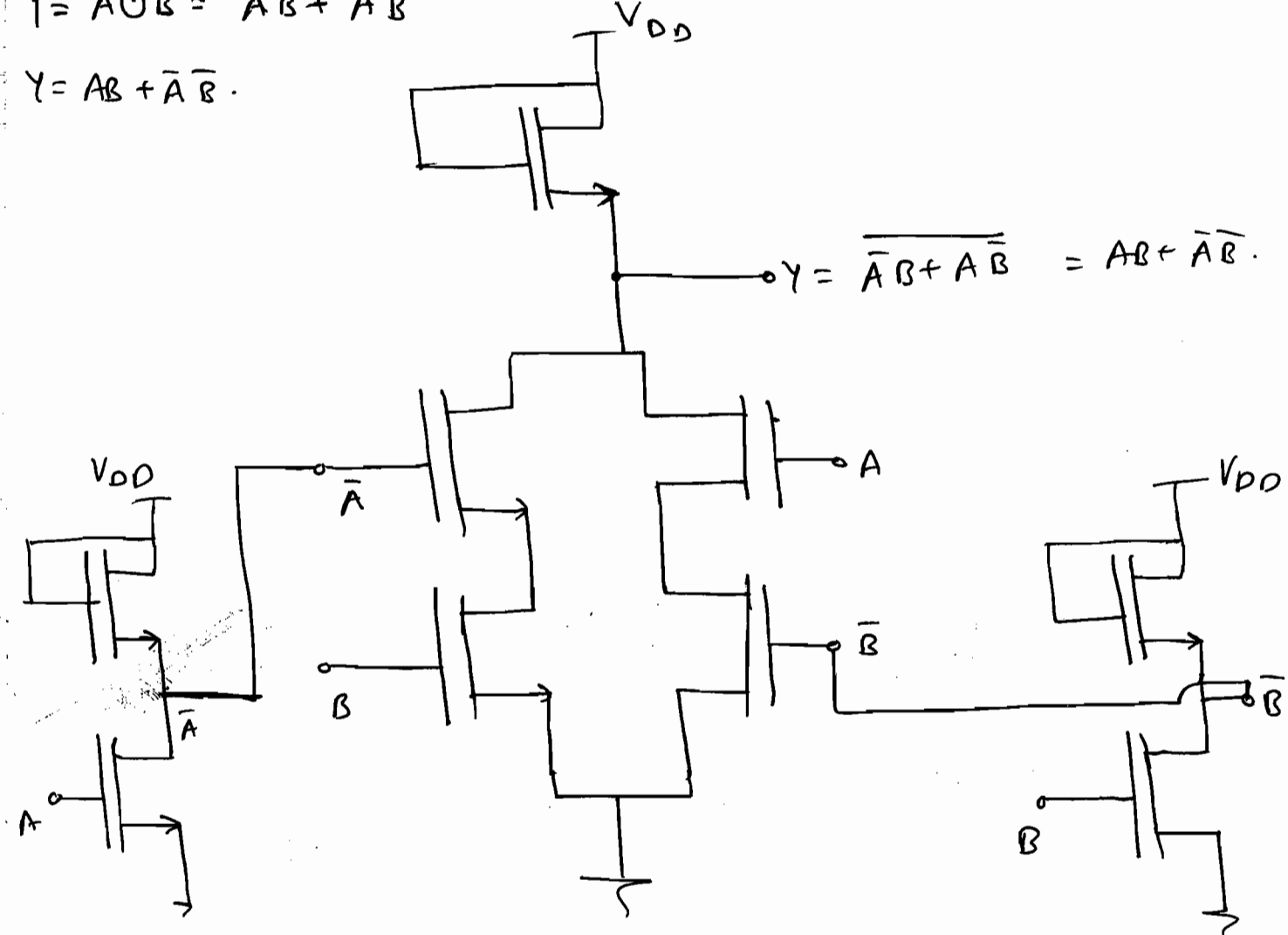
* Nmos:



* 2-i/p ~~XOR~~ XNOR gate:

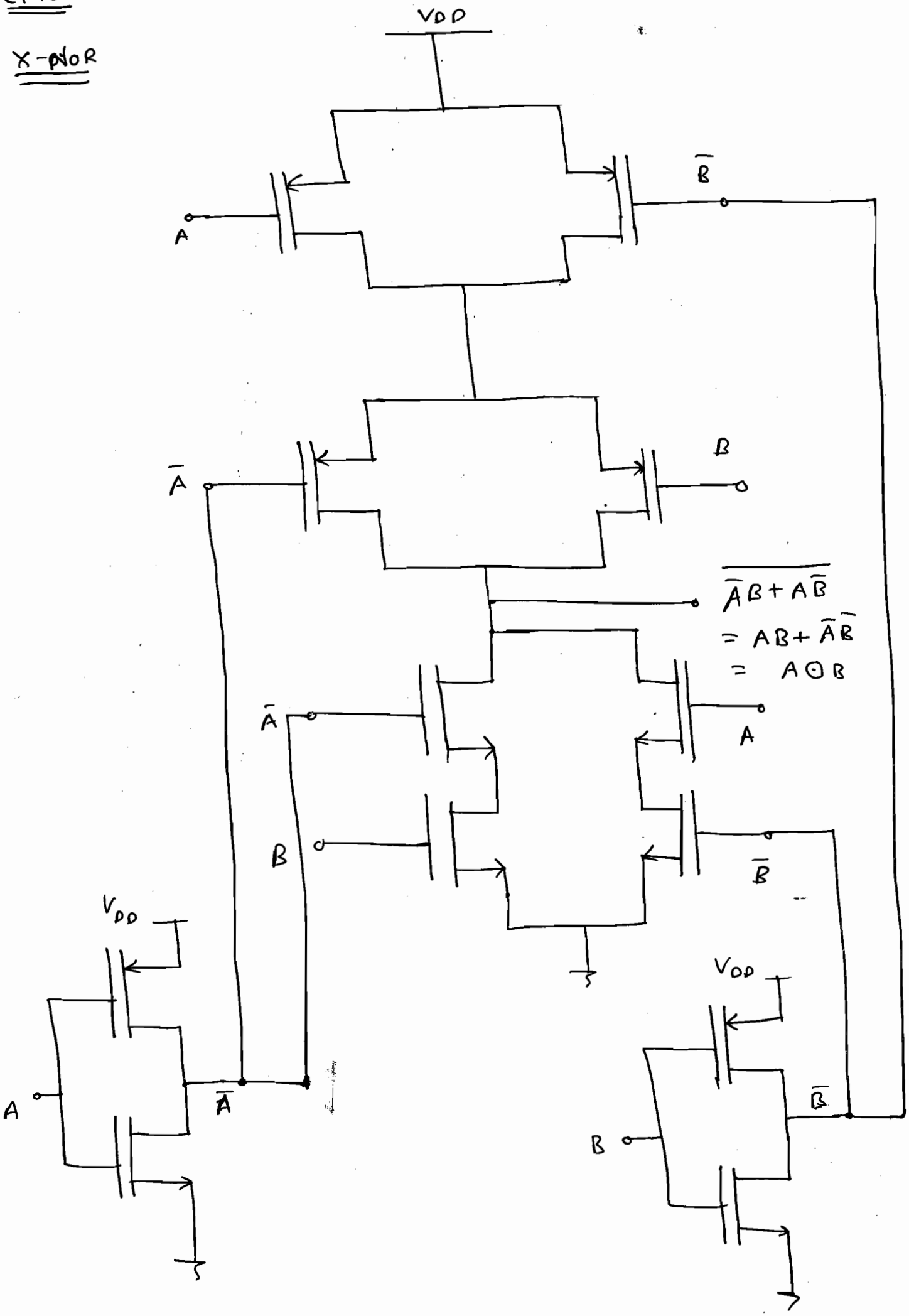
$Y = A \odot B = \overline{\bar{A}B + A\bar{B}}$

$Y = AB + \bar{A}\bar{B}$.



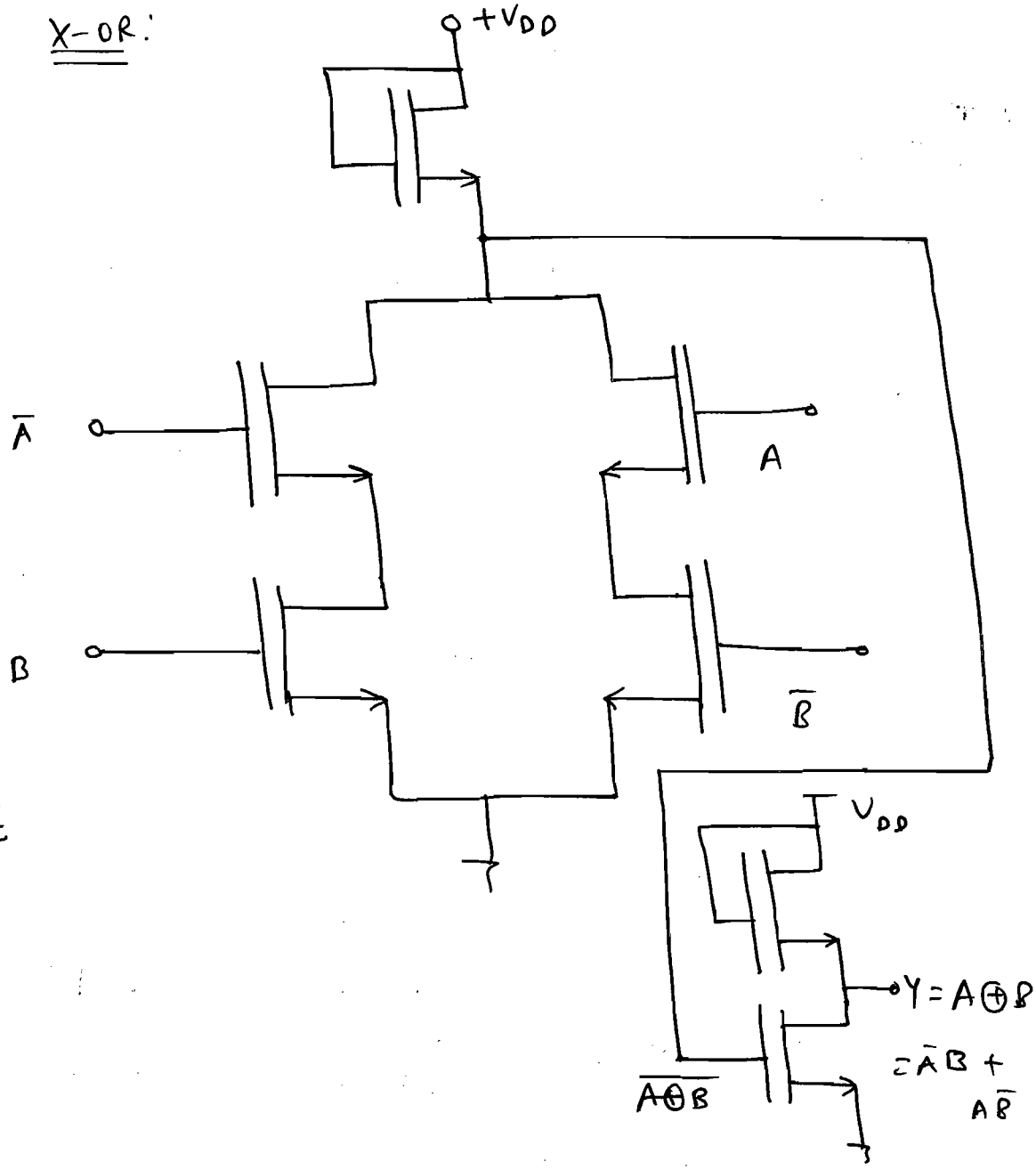
CMOS:

X-NOR


VDD
A
$\bar{B}$
$\bar{A}$
B
$\overline{\bar{A}B + A\bar{B}}$
$= AB + \bar{A}\bar{B}$
$= A \odot B$
$\bar{A}$
A
B
$\bar{B}$
V_{DD}
A
$\bar{A}$
V_{DD}
$\bar{B}$
B

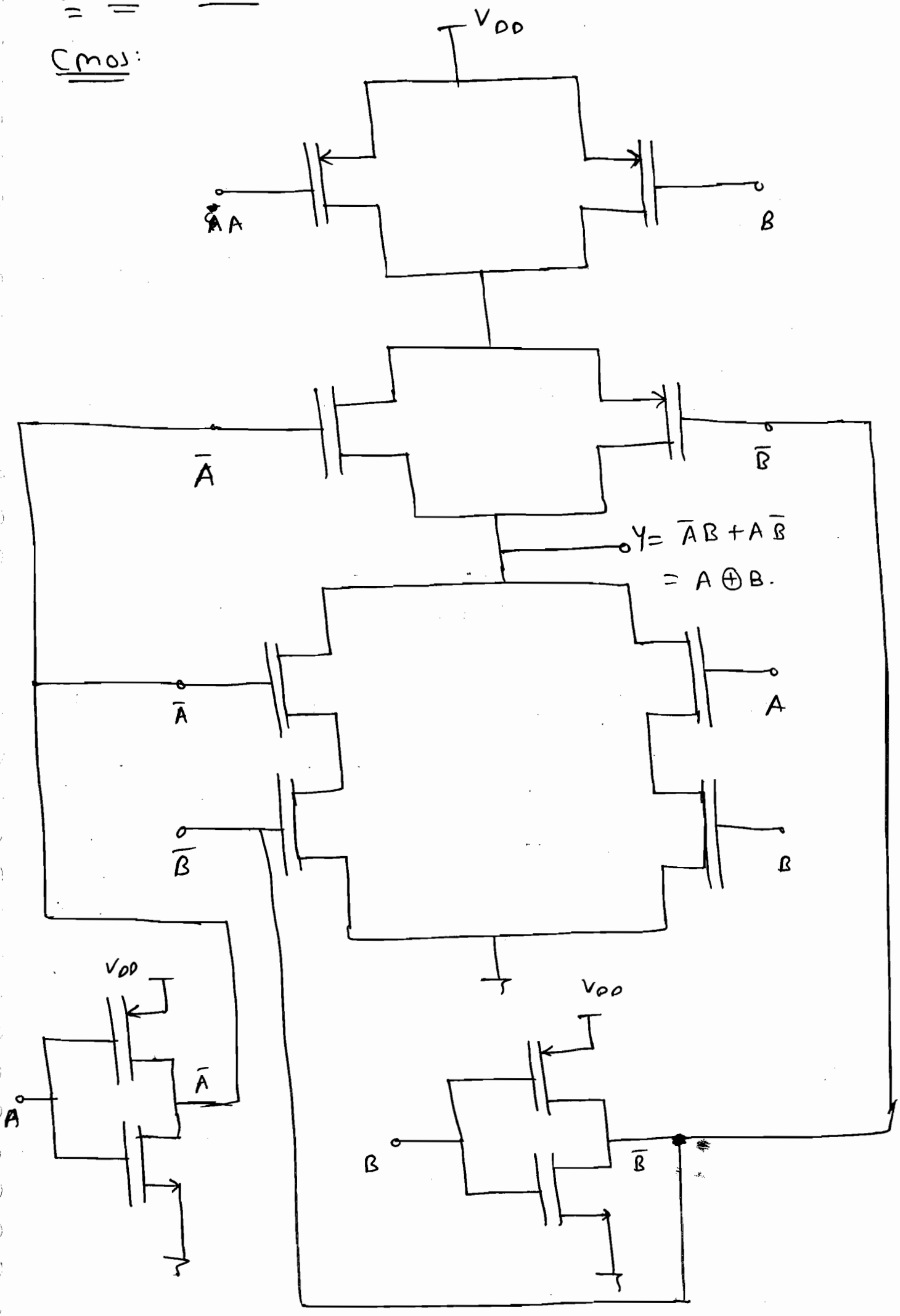
* 2 I/P X-OR:

$Y = \bar{A}B + A\bar{B}$



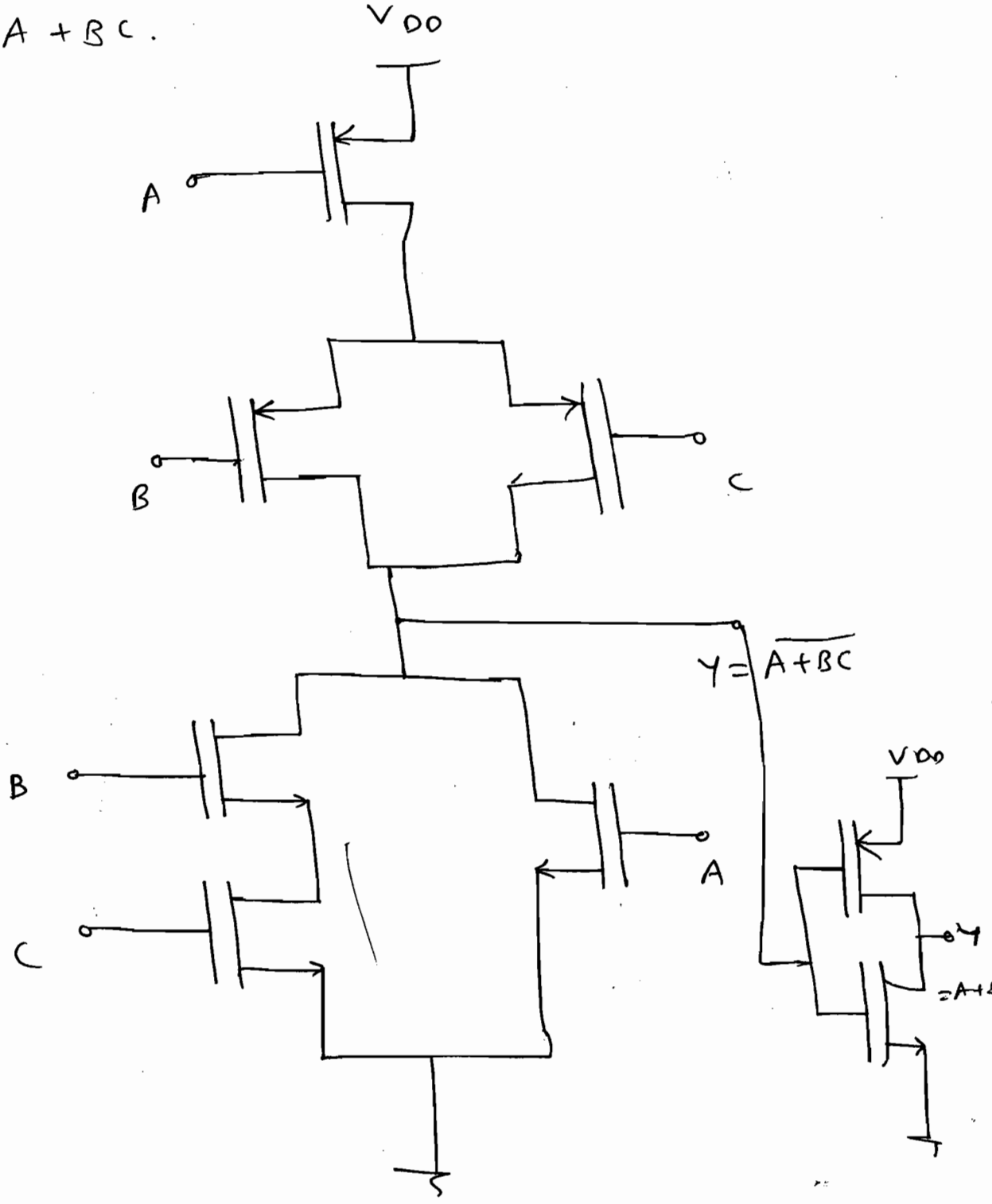
* 2-i/p X-OR :

Cmos:


V_{DD}
A
B
$\bar{A}$
$\bar{B}$
$Y = \bar{A}B + A\bar{B}$
$= A \oplus B.$
$\bar{A}$
A
$\bar{B}$
B
V_{DD}
$\bar{A}$
A
V_{DD}
B
$\bar{B}$

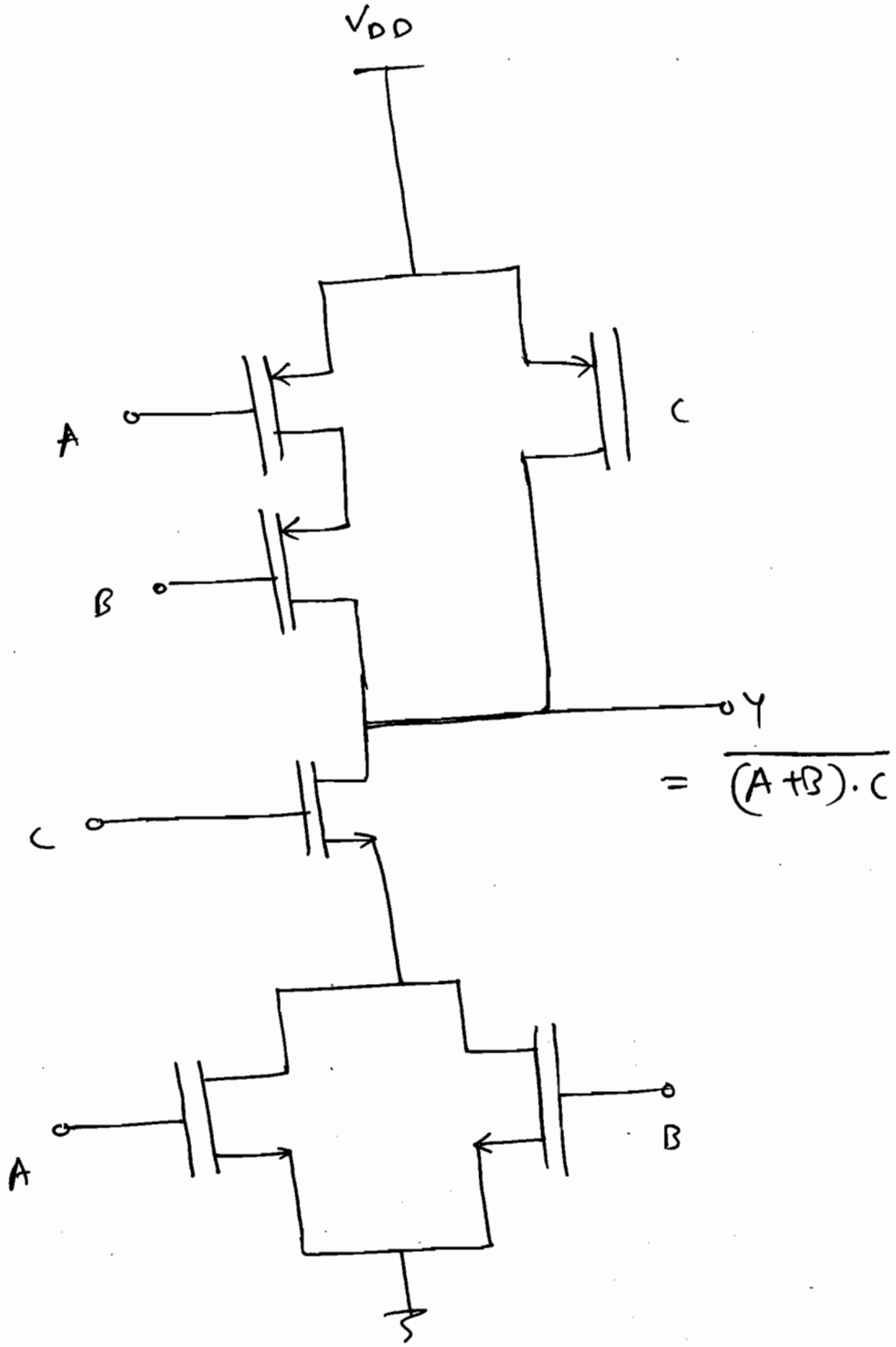
* Implement the following fn in CMOS technology:

① $Y = A + BC$.

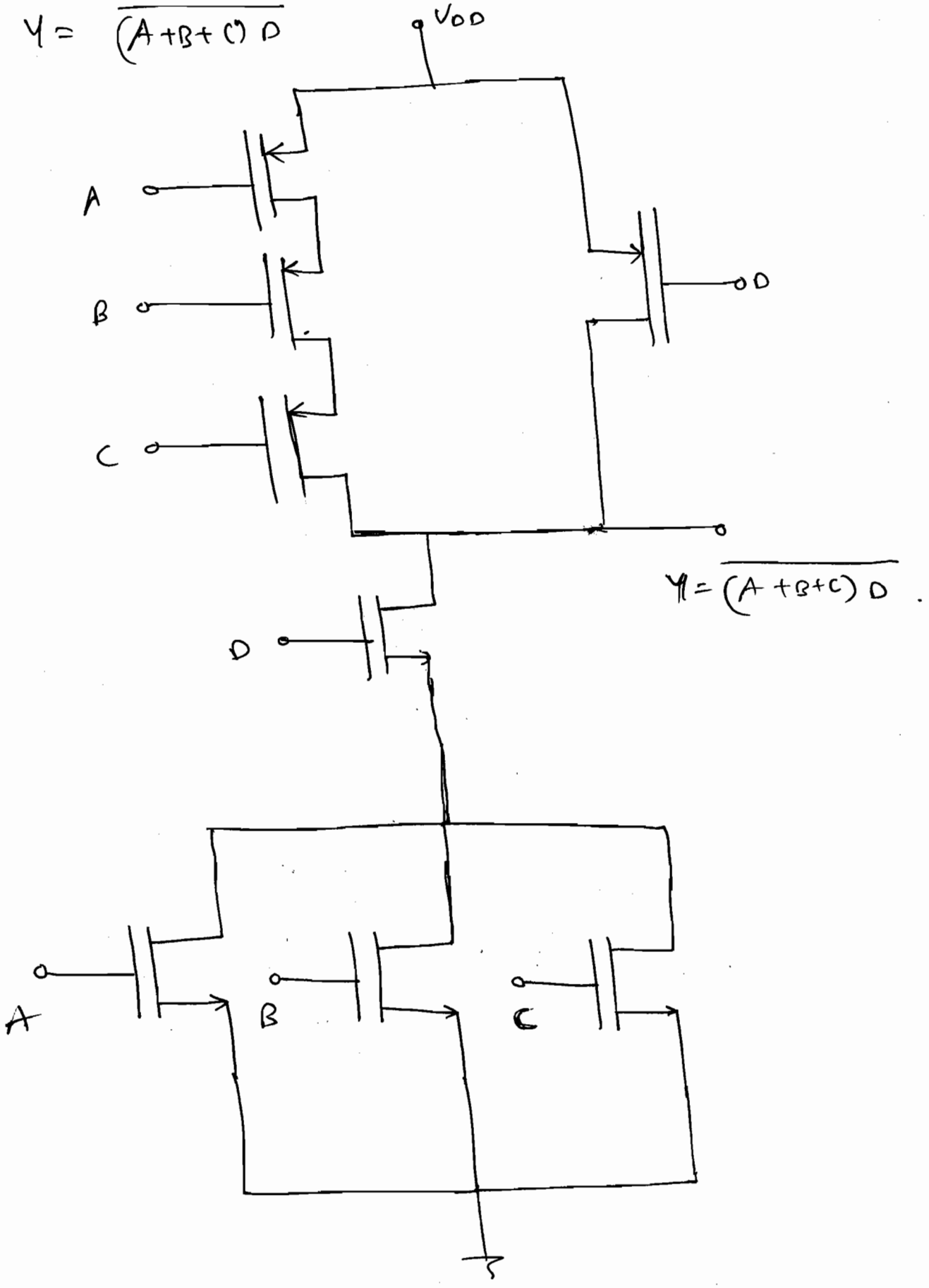


② $Y = \overline{(A+B)\cdot C}$

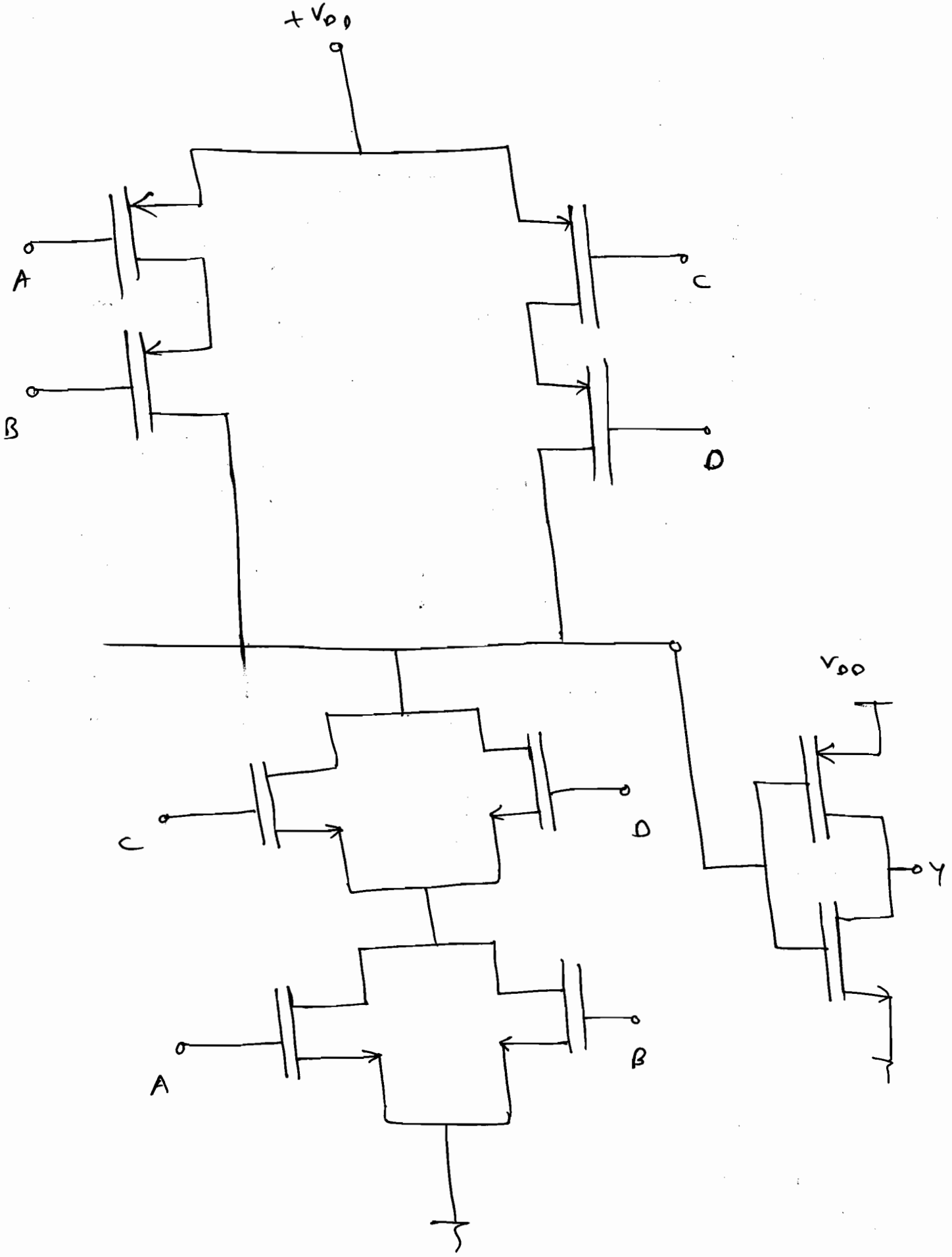
⇒



3. $Y = \overline{(A+B+C)D}$

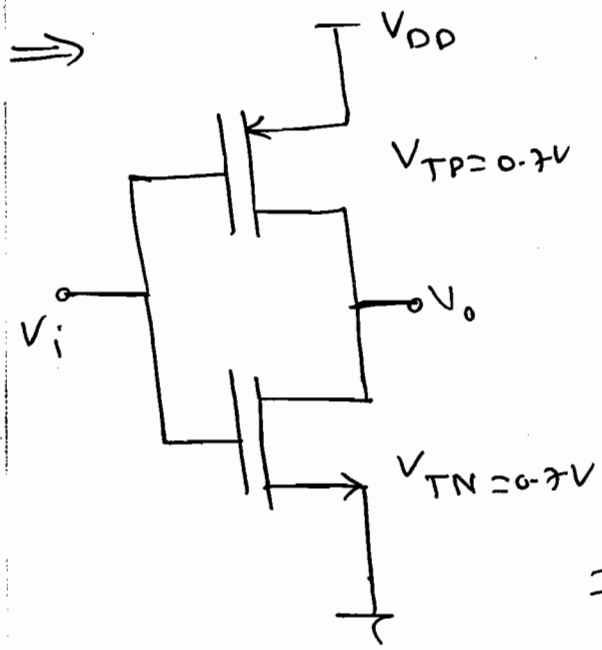


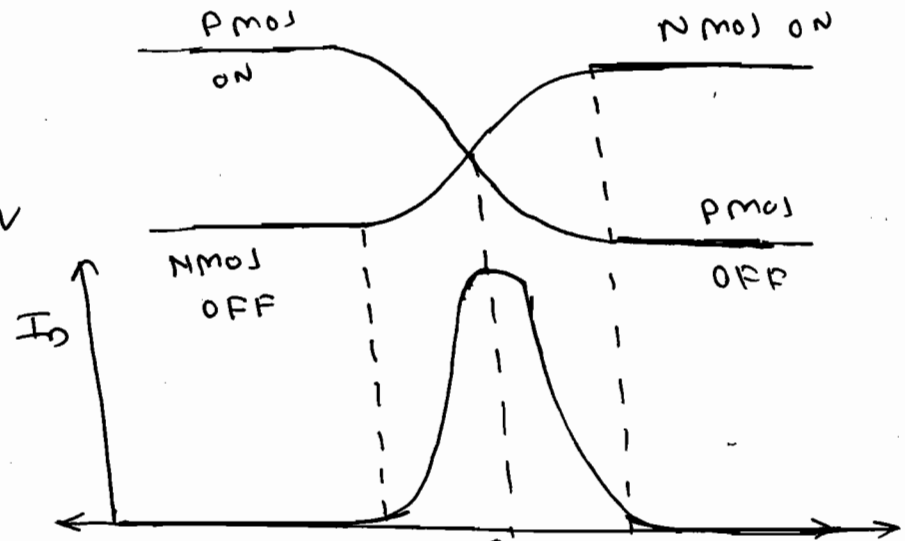
4. $Y = (A+B)(C+D)$.

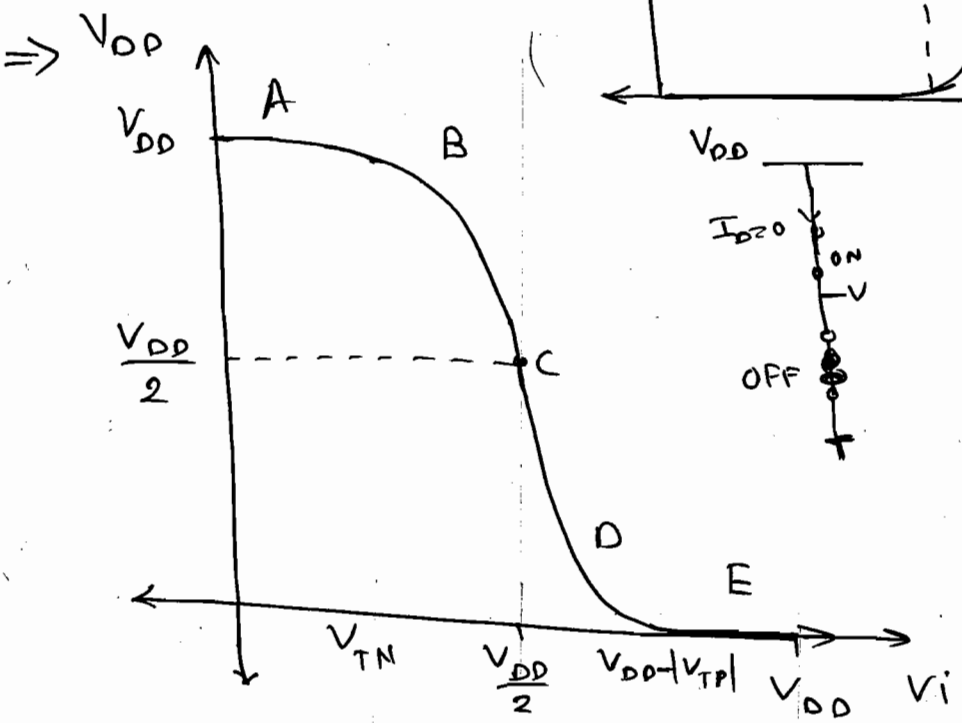


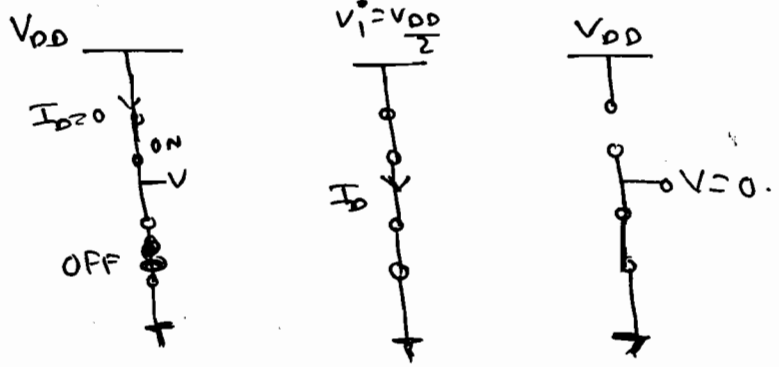
✡ Transfer Characteristics of An Inverter:

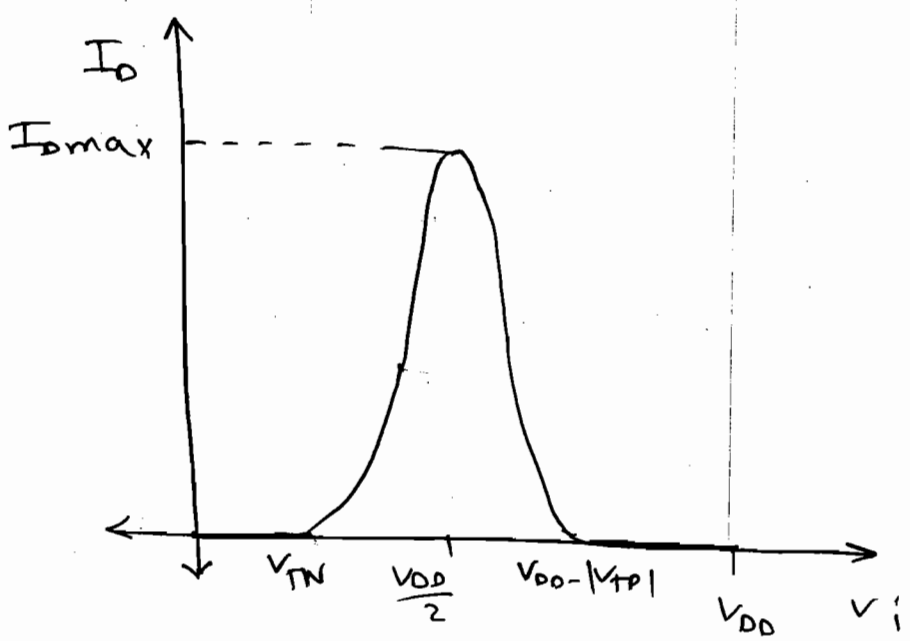
– IMP











Reg	Condition	PMOS	NMOS	output
A	$0 < V_i < V_{TN}$	Linear	cut-off	$V_o = V_{DD}$
B	$V_{TN} < V_i < V_{DD}/2$	Linear	Sat	$V_o > \frac{V_{DD}}{2}$
C	$V_i = V_{DD}/2$	Sat	Sat	V_o drops sharply
D	$\frac{V_{DD}}{2} < V_i < V_{DD} - \lvert V_{TP}\rvert$	Sat	Linear	$V_o < V_{DD}/2$
E	$V_i > V_{DD} - \lvert V_{TP}\rvert$	cut-off	Linear	$V_o = 0$

① $0 < V_i < V_{TN}$. ∴

NMOS

$\Rightarrow V_i = 0.5\,V$

$V_{GS} = V_G - V_S$

$V_{GS} = 0.5$

$V_{GS} = 0.5 < (V_{TN} = 0.7V)$

So, OFF

PMOS

$V_i = 0.5\,V$

$V_{GS} = V_G - V_S$

$= 0.5 - 5 = -4.5$

$\therefore V_{GS} = -4.5 < V_{TP}$.

Now, $V_{DS} = V_D - V_S$

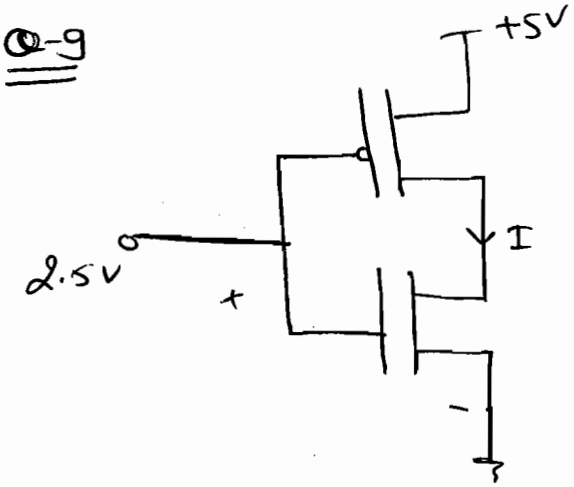
$= V_{DD} - V_{DD} = 0$

$V_{DS} = 0$.

$V_{GS} - V_T = -4.5 - (-0.7) = -3.8 < V_{DS}$.

$V_{DS} > V_{GS} - V_T \Rightarrow$ linear.

Q-9



$K_n = K_p = \mu_n C_{ox} \cdot \frac{W_n}{L_n}$.

$= \mu_p \cdot C_{ox} \cdot \frac{W_p}{L_p} = 40\,\mu A/V^2$

$V_{GS} = 2.5V$

$V_T = 1.V$

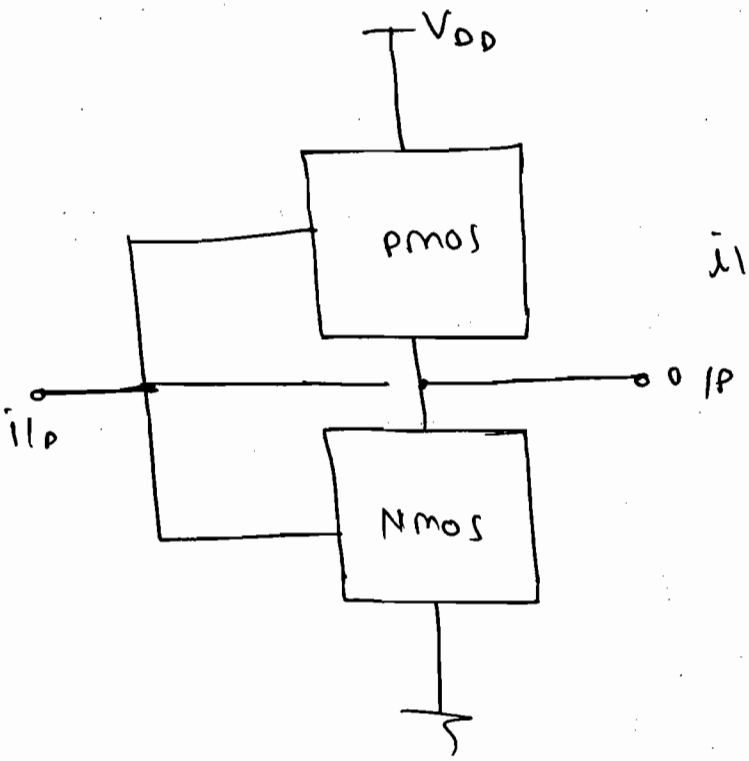
Soln

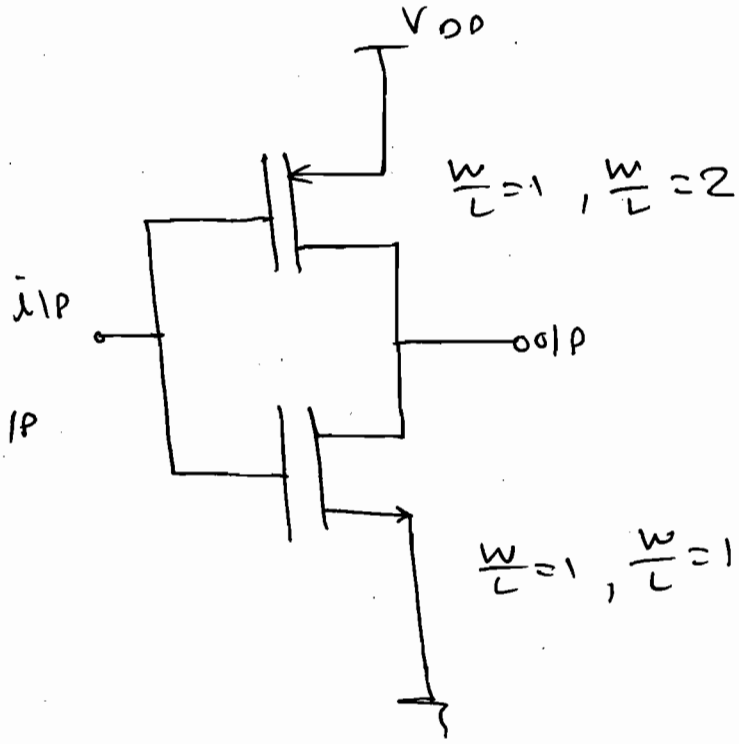
$I_D = \frac{1}{2} \mu_n C_{ox} \cdot \frac{W_n}{L_n} [V_{GS} - V_T]^2$

$= \frac{1}{2} \times 40 \times 10^{-6} [2.5 - 1]^2 = 20 \times 10^{-6} \times 2.25$

$\boxed{I = 45\,\mu A}$

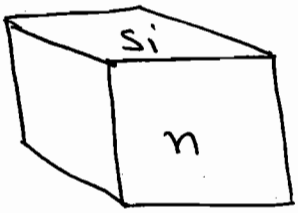
* Transistor sizing:

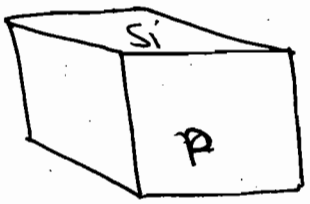




n-mos	pmos
$L = 1\ \mu m$	$L = 1\ \mu m$
$\omega = 1\ \mu m$	$W = 1\ \mu m$.

$\Rightarrow$





$\sigma_n = n \mu_n q$ $\qquad$ $\sigma_p = n \mu_p q$

Si

$\rightarrow \mu_n = 1300 \ cm^2/V\text{-}s$

$\mu_p = 500 \ cm^2/V\text{-}s$

$\therefore \mu_n > 2\mu_p$

$\therefore \mu_n \simeq 2\mu_p$

$\Rightarrow \sigma_n = 2\sigma_p$

$\therefore \rho_p = 2\rho_n.$

$\therefore R_n = \dfrac{\rho_n L}{A}$

$\downarrow R_p = \dfrac{\rho_p L}{A \uparrow}$

$\therefore R_p = 2R_n.$

for $R_p = R_n$

$\therefore A_p = 2A_n$

$\Rightarrow \boxed{\left(\frac{W}{L}\right)_p = 2\left(\frac{W}{L}\right)_n.}$

⇒ nMOS

$L = 1\,\mu m$

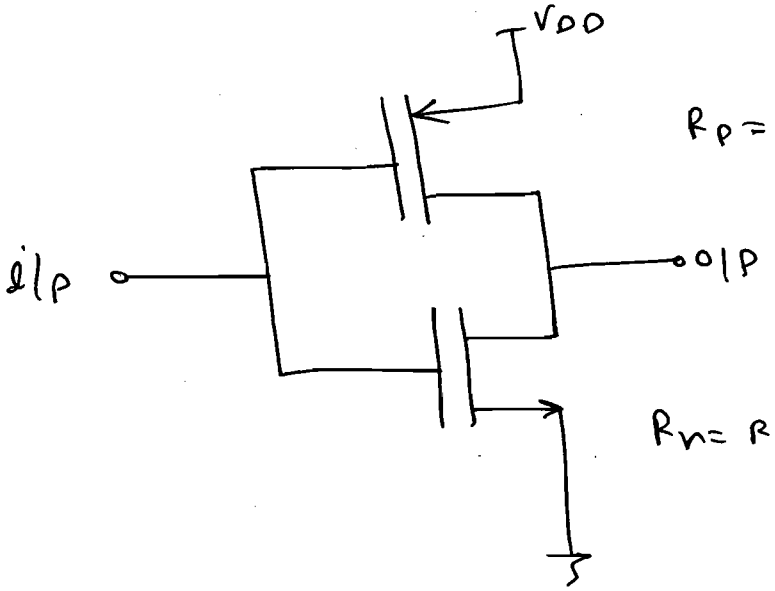
$W = 1\,\mu m$

PMOS

$L = 1\,\mu m$

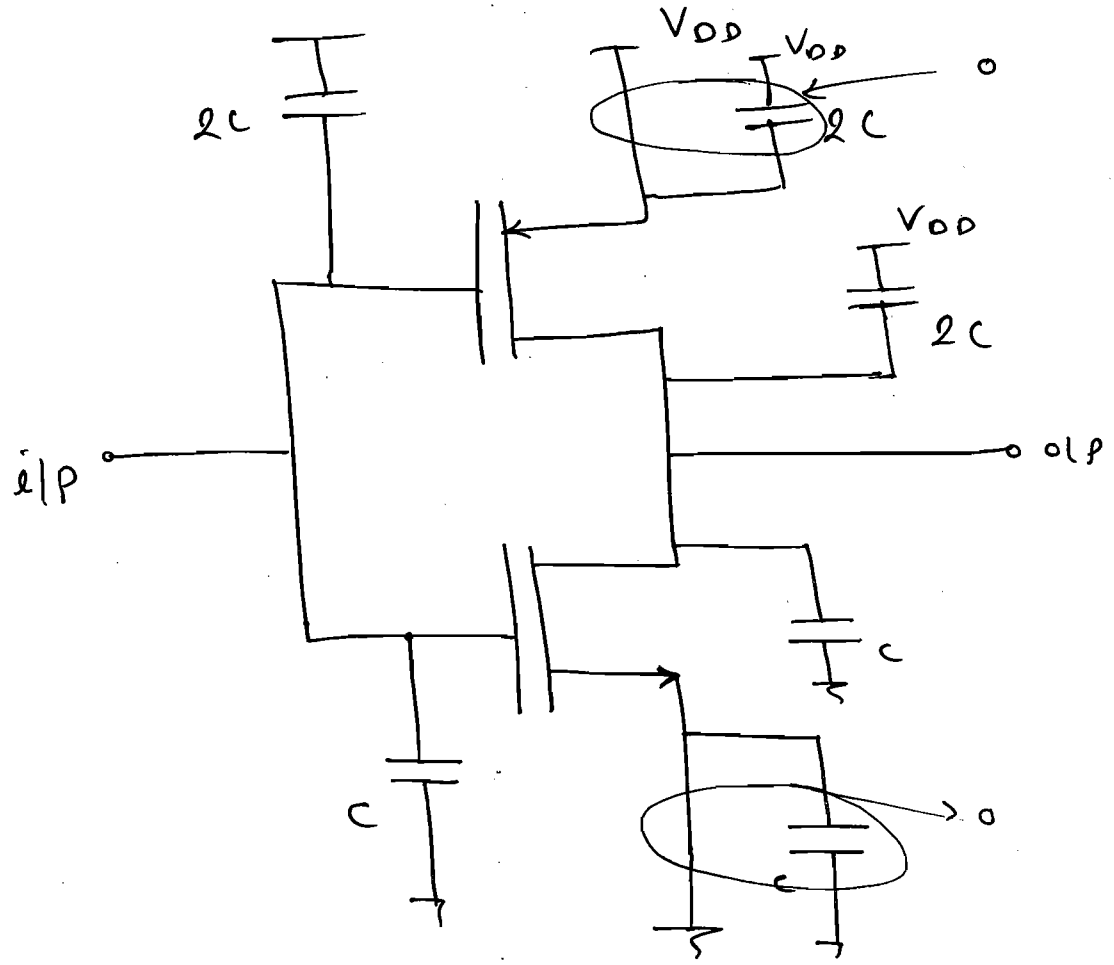
$W = 2\,\mu m$

*



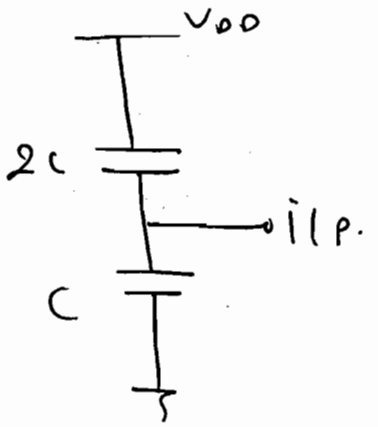
$R \propto \frac{1}{(W/L)}$:

*

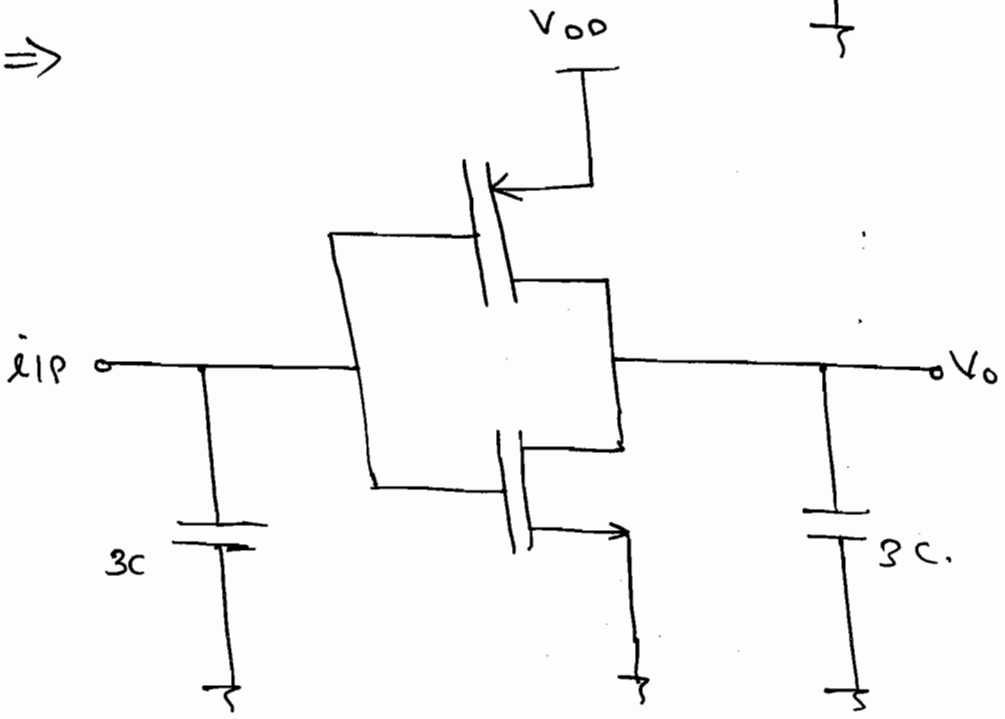


$\left(C \propto \frac{W}{L}\right)$

⇒ i/p capacitance,



⇒

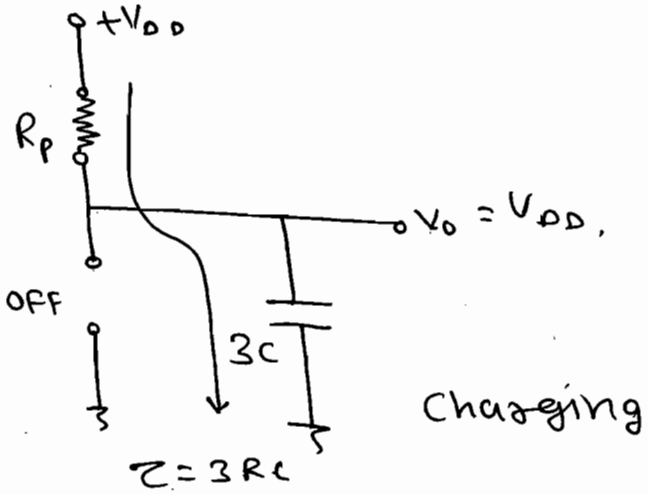


⇒ ① $V_i = 0$

⇒ NMOS : OFF

⇒ PMOS : ON

Rise time $(t_{pdr}) = 3CR_p$.

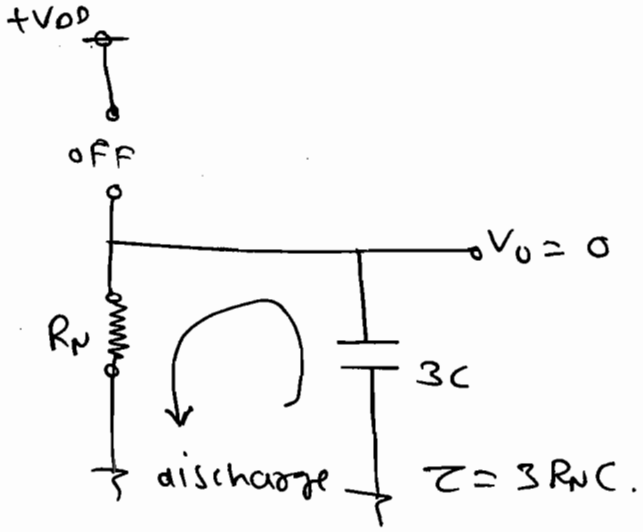


⇒ ② $V_i = V_{DD}$.

⇒ NMOS : ON.

⇒ PMOS : OFF.

Fall time $(t_{pdf}) = 3R_nC$.

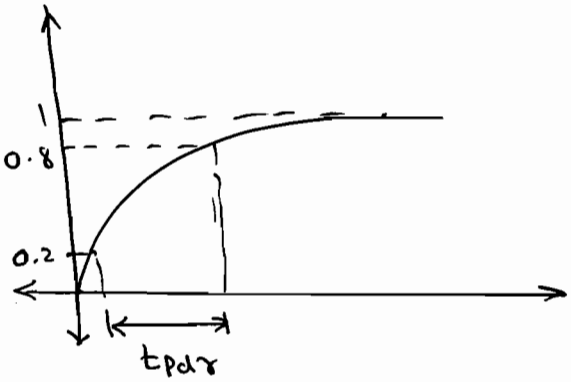


* Propogation Delay:

$$(t_{pd}) = \frac{t_{pdr} + t_{pdf}}{2}$$

* Rise - time (t_{pdr}) : (t_r)

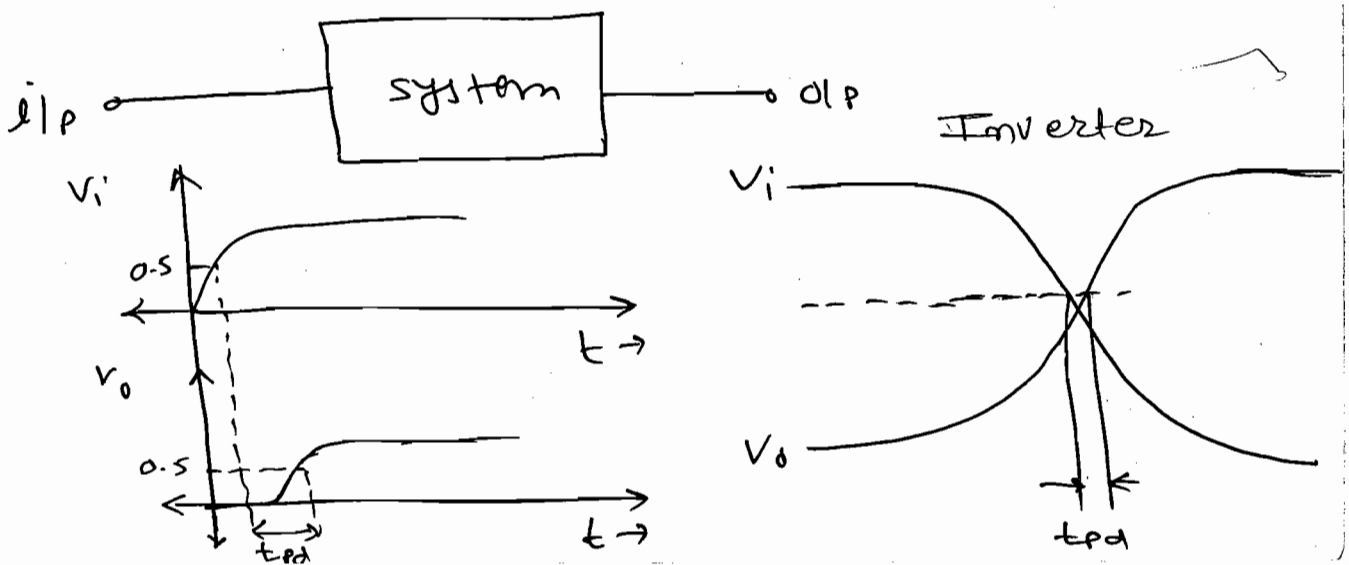
⇒ It is the time taken by the waveform to rise from 20 % to 80 % of its steady state value.



② Fall time (t_f):

⇒ It is the time taken by the waveform to fall from 80 % to 20 % of its steady state value.

③ Propogation delay (t_{pd}):



⇒ it is the max. time from the i/p crossing 50 % to the o/p crossing 50 %.

④ Contamination Delay : (t_{cd}):

⇒ It is the minimum time from the input crossing 50 % to the o/p crossing 50 %.

☆ Power Calculation::

1. Dynamic Power 2. Static Power.

① Dynamic Power. :-

⇒ Dynamic power is the power consumed by the MOSFET during its transition. i.e. it is the power consumed by the MOSFET during switching (or) Tansition from Logic '1' to Logic '0' (or) from Logic '0' to Logic '1'.

(i) Capacitor charging & discharging power.

(ii) Short ckt Power & Crowbar Power.

(i) Capacitor Charging & Discharging power.:

⇒ The energy dissipated across the ~~Capacitor~~ P-mos transistor during capacitor charging,

$$E_c = \frac{1}{2} C V_{DD}^2.$$

(C ← total capacitance)

⇒ The energy dissipated across the nmos transistor during discharging

$$E_D = \frac{1}{2} C \cdot V_{DD}^2.$$

(C ← total capacitance)

⇒ Total energy dissipated across PMOS & nmos Transistors $= E_D + E_c$

$$\therefore E = CV_{DD}^2.$$

$$\therefore \text{Power } P = \frac{E}{T} = \frac{CV_{DD}^2}{T}.$$

(T ← Time period of switching)

$$\therefore P = CV_{DD}^2 \cdot f.$$

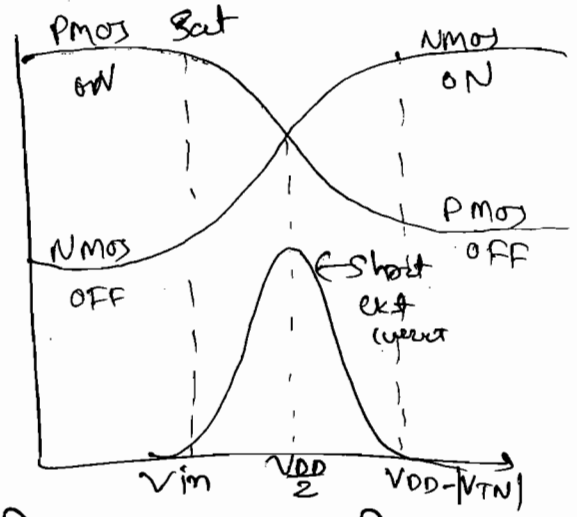
(f ← freq^n of switching)

$$\therefore \boxed{P_{\text{charg \& discharg}} = CV_{DD}^2 \cdot f}$$

(ii) Short Ckt power :-

Reg	Cond^n	PMOS	NMOS
C	$V_i = \frac{V_{DD}}{2}$	Sat	Sat

P_{short}



⇒ Total Dynamic Power $= P_{\text{charg \& dischg}} + P_{\text{short ckt}}$

$\approx P_{\text{charg \& dischar.}}$

$$\boxed{P_{\text{dynamic}} = CV_{DD}^2 \cdot f.}$$

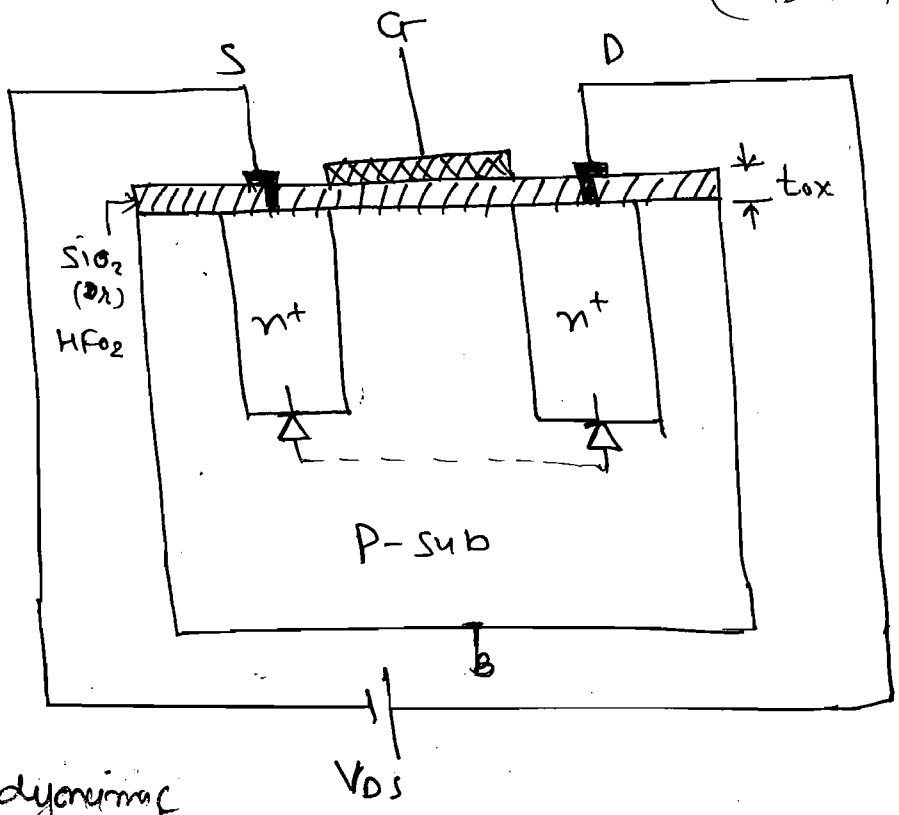
(2.) Static Power:

⇒ Static power is the power consumed by the MOSFET during ideal state i.e. it is the power consummed by the MOSFET during continuously ON at Logic '1' state (or) continuously OFF Logic '0' state. & this is due to

(i) Gate oxide leakage Current. ($I_{gleakage}$).

(ii) junction leakage current. ($I_{jleakage}$).

(iii) Subthreshold leakage current. ($I_{subleak}$).
($V_{GS} < V_T$)



$\epsilon_{SiO_2} = 3.9$

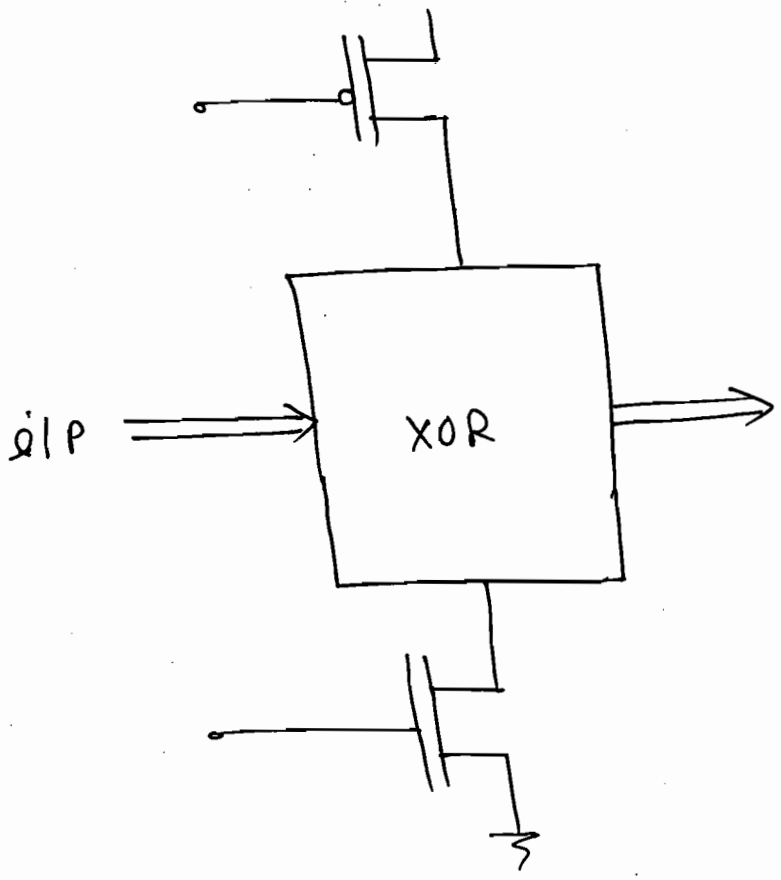
$\epsilon_{HfO_2} = 30.$

up to 90nm
$P_{dynamic} > P_{static}$
below 90nm
$P_{static} > P_{dynamic}$

⇒ $P_{static} = \left(I_{gateleak} + I_{junleak} + I_{subleak}\right) V_{DD}.$

∴ $\boxed{P = P_{dynamic} + P_{static}.}$

⇒



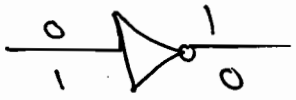
⇒ speed decreases but Static & leakage power dissipation decreases

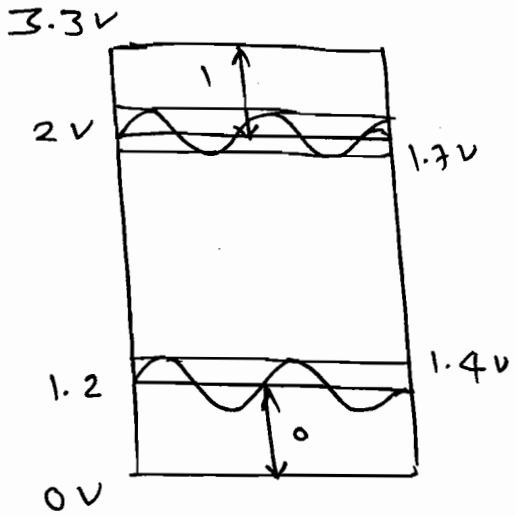
⇒ Low power VLSI Technology

* Noise Margin:

⇒ Noise Margin allows you to determine maximum allowable noise voltage at the input of the gate without disturbing output.

⇒





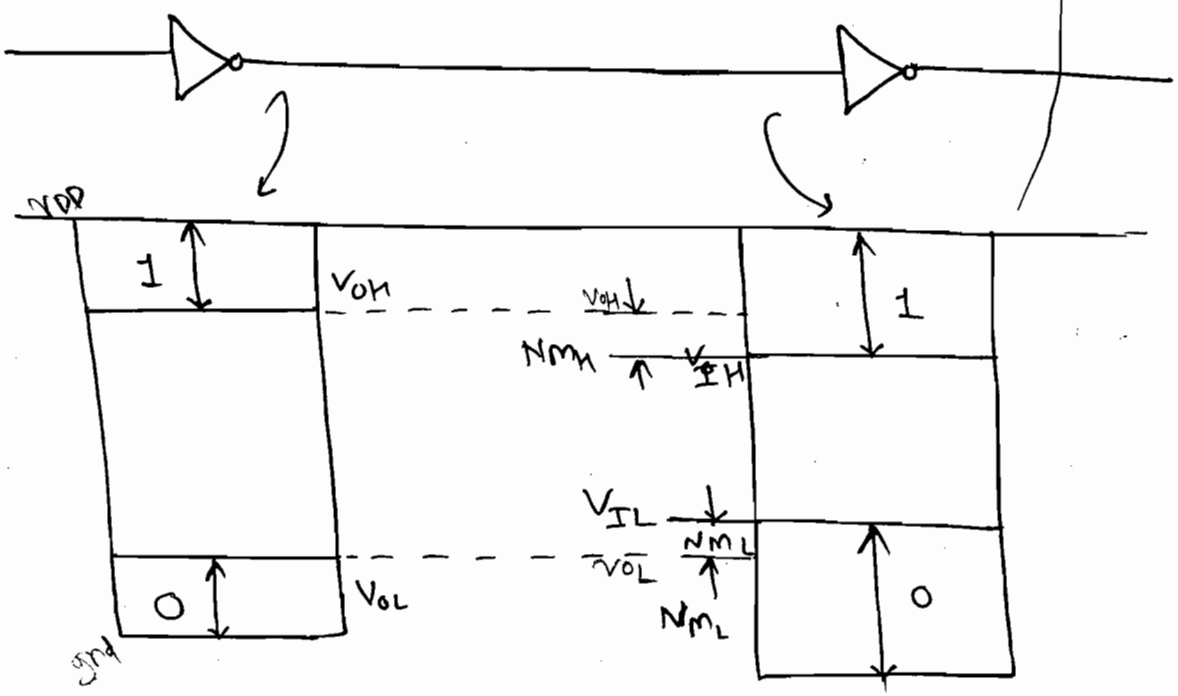
① High Noise Margin. (NMH):

$$NM_H = V_{OH} - V_{IH}$$

② Low Noise Margin. (NML):

$$NM_L = V_{IL} - V_{OL}.$$

⇒



→ V_{OH}: ~~Max~~. Min. High o/p voltage.

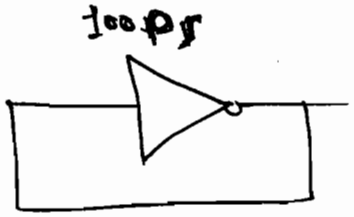
V_{IH}: ~~Max~~. ~~High~~ Min. High I/p Voltage.

V_{OL}: Max. Low o/p Voltage.

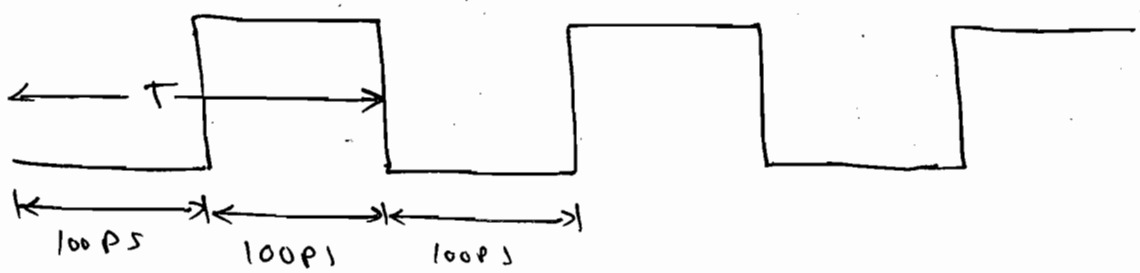
V_{IL}: max. Low I/p voltage.

⇒ $V_{OL} < V_{IL} < V_{IH} < V_{OH}$.

⇒



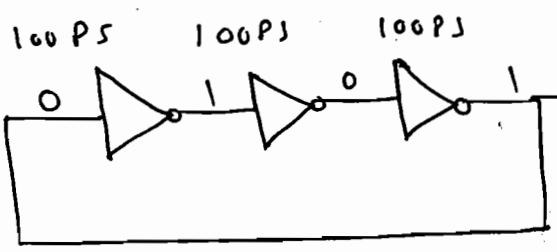
$V_0 = 0$ ⌐ 100PS
$= 1$ ↵
$= 0$ ⌐ 100 PS
$= 1$ ⌐ 100 PS.
$= 0$ ⌐ 100 PS.



$T = 200\,PS.$

$f = \frac{1}{200P}\ Hz$

$\Rightarrow$



Ring oscillator

$V_0 = 0$] 300PS

$V_0 = 1$

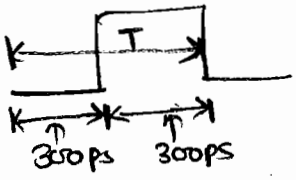
$V_0 = 0$] 300PS

$V_0 = 1$] 300PS.

$T = 600ps$

$f = \frac{1}{600ps}$

$\therefore$ $\boxed{f_0 = \frac{1}{2Nn}}$



$\Rightarrow$ N = no. of inverter

n = delay of each inverter.

$\therefore f_0 = \frac{1}{2 \times 3 \times 100} = \frac{1}{600P}\ Hz.$

applicable only for same time delay for every inverter & numng inverter is added

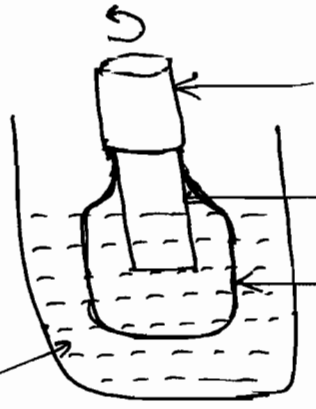
☆ Device Technology :-

1. Crystal growth and wafer Preparation.
2. oxidation. ② → Epitaxy
3. Photolithography.
4. Diffusion.
5. Ion - Implantation.
6. Metallization.
7. Passivation.
8. Packing.

(1) Crystal growth and wafer prep.

⑤ Vacuum evaporation of aluminium

⇒ Czochralski Process :

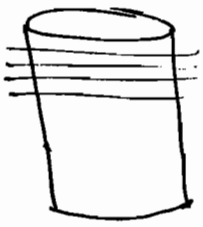


1425°C

growth rate 30 - 180mm/hour

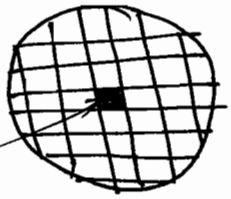
100 cm → length

15 cm → Diameter



Silicon Ingot

wafer

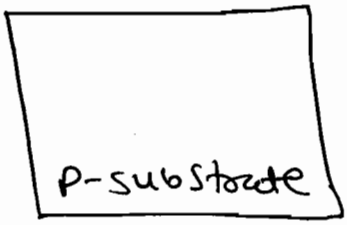


wafer 100 - 8000 Ic

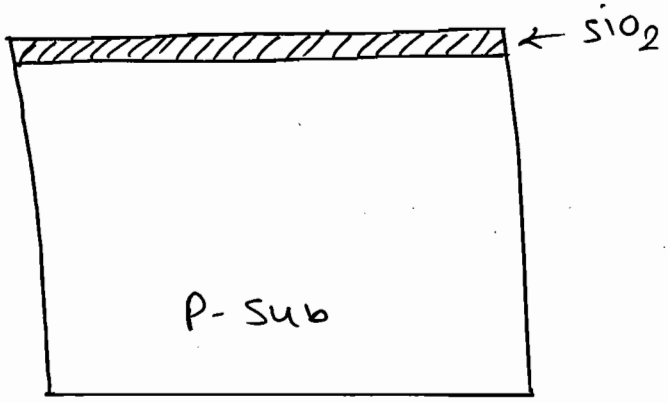
⇒ wafer thickness = 16 to 32 mil.

1 mill ≃ 25 μm

⇒ Diameter : 75 to 300mm.



(2) oxidation:



$Si + O_2 \longrightarrow SiO_2$.

⇒ It is easy to form SiO_2 on top of the Silion without adding any extra material.

⇒ It doesn't allow any impurity through it.

⇒ It disolve only in Hydrochloric Acid.

⇒ SiO_2 is a dielectric material therefore it can be used as a insulator (or) isolator betⁿ two devices (or) two stages.

⇒ There are two methods of oxidation:

① Dry oxidation:

⇒ $Si + O_2 \longrightarrow SiO_2$.

→ take place at 1200°C.

→ Slow Process.

→ Thin layers.

→ Dry oxidation is a Slow Process. But

the electric properties of Dry oxidation is better than wet oxidation.

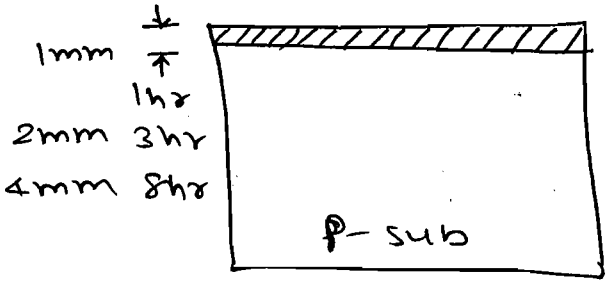
(ii) Wet oxidation:

→ $Si + 2H_2O \longrightarrow SiO_2 + H_2O$.

→ 900° to 1000°C

→ Fast

→ thick layers.



(iii) Photolithography:

⇒ Photo → ~~picture~~ lights

lithos → Stone

graphy → picture.

→ (i) Photoresist ✓

(ii) Photo mask. ✓

(iii) UV rays. ✓

(iv) Developing ✓

(v) Etching.

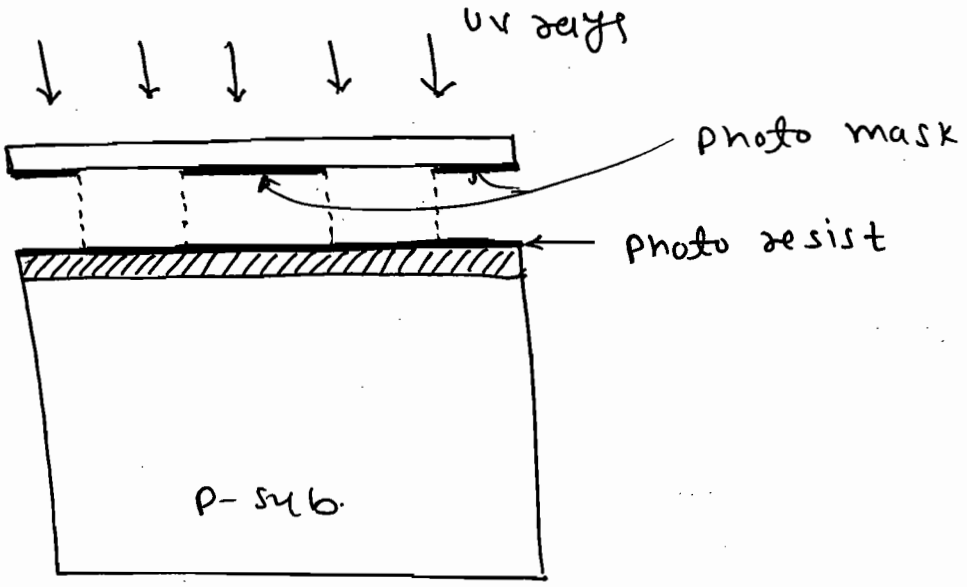
(vi) Stripping.

⇒ Stripping is a process of removing uncoated portion.

⇒ Photo resist:

① Positive photo resist ② Negative Phto resist.

⇒



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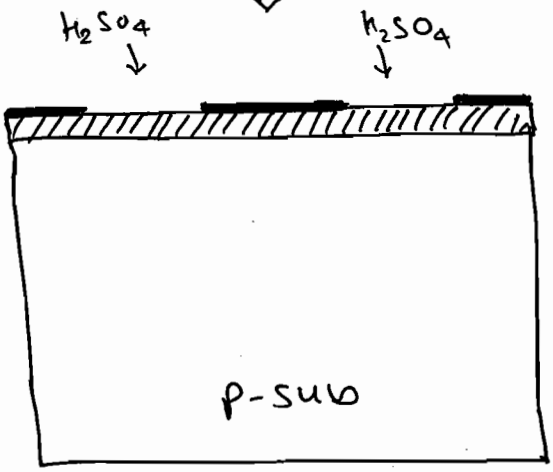

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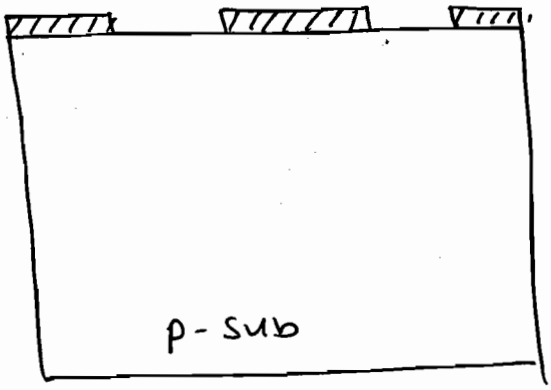
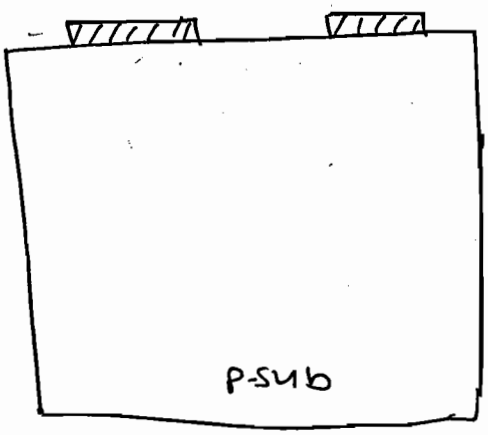




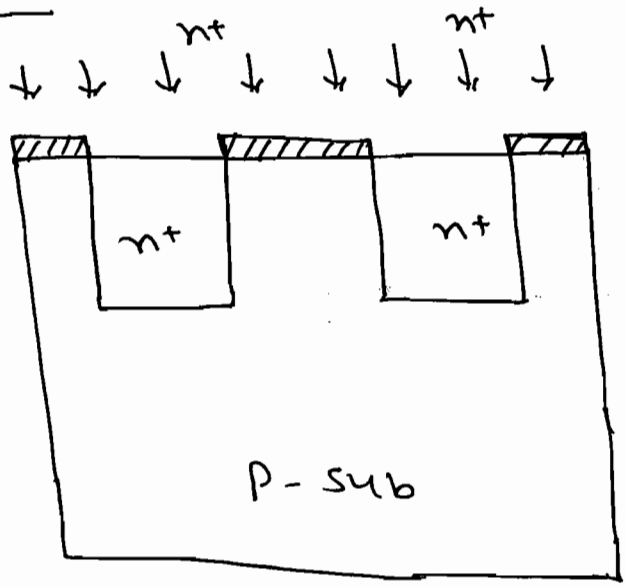
positive photo resist

negative photo resist.

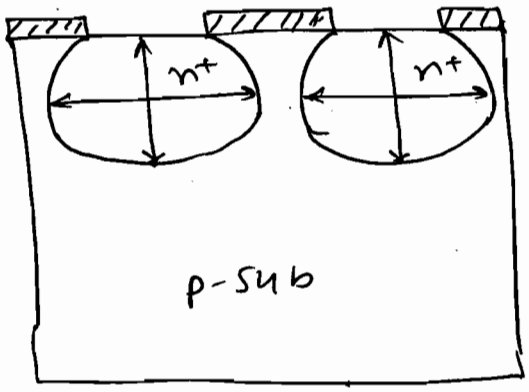
⇒ The portion of the silicon dioxide which is exposed to uv rays if it gets removed during etching process then it is called positive photo resist.

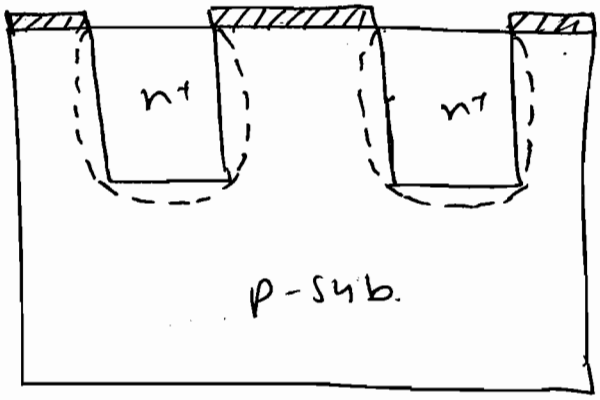
⇒ The portion of the silicon dioxide which is not exposed to UV rays it gets removed during etching then it is called -ve photo resist.

(4) Diffussion:



(i) Isotropic diffusion: (ii) Anisotropic diffusion:





⇒ Take place: 1000°C

⇒ for n+ type: P_2O_5, $POCl_3$ (Phosphorus oxi Cloride).

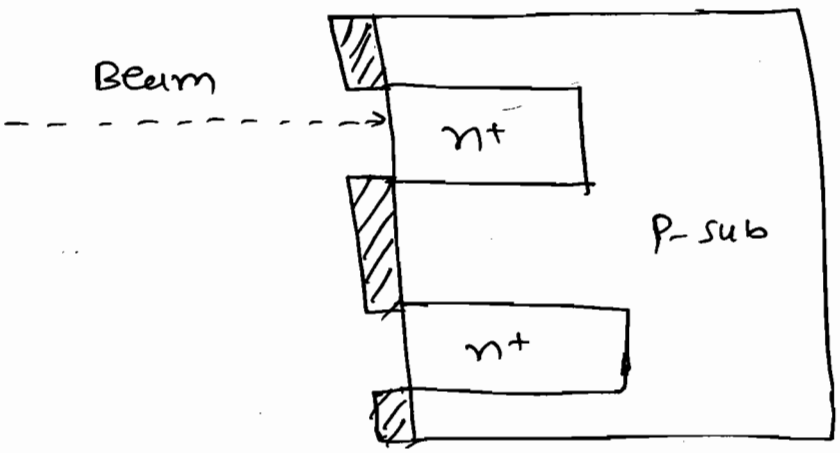
⇒ for p+ type: BrO_3, BCl_3.

(SBO)

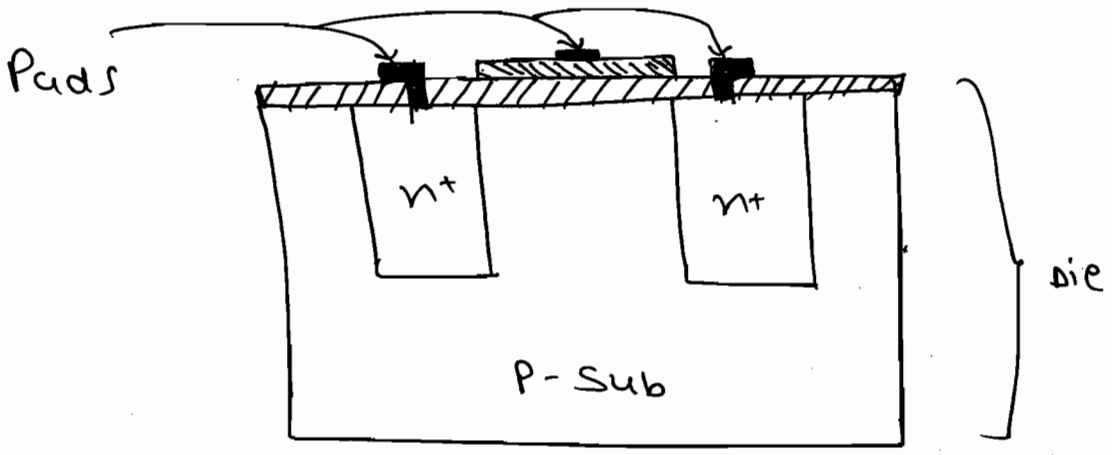
(5) Ion - Implantation:

⇒ It is also same as diffusion process but it take place at lower temperature and slow process.

⇒



(6) Metallization:



⇒ Metallization is a process of forming metallic contact bet^n the device for inter connection.

⇒ Old design : Al

⇒ New design : Cu

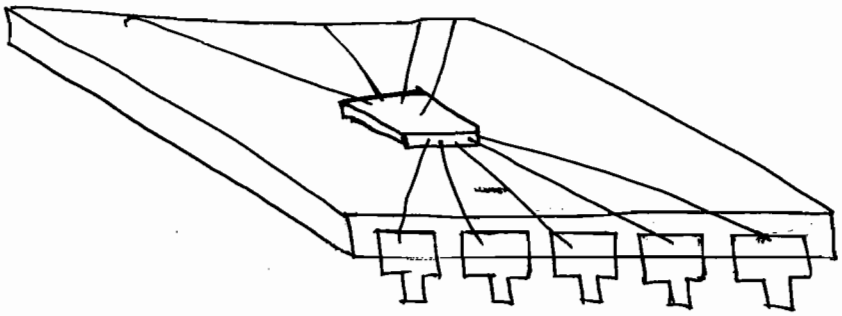
$(\sigma_{Cu} > \sigma_{Al})$ ⇒ to reduce contact resistance.

(7.) Passivation:

⇒ Passivation is a process of forming glass type of epoxy coating on the surface of the die to protect it from the atmosphere and also to provide mechanical strength.

(8) Packing:

⇒ Die: 10 to 20%.



→ more than 200 types of packing.

→ DIP package.

→ PLC, QFN

→ PGA (pin grid array).

→ BGA (Balls grid array)

↑
Low power like memories, µP.